Scientific Report (2018-2022)

Competition:	**Complex Ground-Breaking Research Projects_PCCF 2016**
No. of the contract:	PN-III-P4-ID-PCCF-2016-0033
Research domain:	Exact sciences and engineering
Title:	Advanced nanoelectronic devices based on graphene/ferroelctric heterostructures
Acronym:	GRAPHENEFERRO
Duration (months):	48 (July 2018-June 2022)
Project web page:	https://www.imt.ro/grapheneferro/
Host institution: (CO)	INSTITUTUL NATIONAL DE CERCETARE- DEZVOLTARE PENTRU MICROTEHNOLOGIE - IMT BUCURESTI INCD
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Project partner 1 (P1):	UNIVERSITATEA DIN BUCURESTI, Facultatea de Fizică, Măgurele
Project partner 2 (P2):	INSTITUTUL NATIONAL DE CERCETARE - DEZVOLTARE PENTRU FIZICA MATERIALELOR BUCURESTI - Măgurele
Project partner 3 (P3):	INSTITUTUL NATIONAL DE CERCETARE DEZVOLTARE PENTRU FIZICA LASERILOR, PLASMEI SI RADIATIEI - INFLPR -Măgurele

The objectives of the period (2018-2022)

Motivation

A large number of present-day applications, such as high-frequency, neuromorphic and logic circuits and energy harvesting systems require tunable and reconfigurable functionalities. The GRAPHENEFERRO project deals with electronic devices and circuits based on graphene/ferroelectric heterostructures, where both materials forming the heterostructure are tunable, i.e., certain physical parameters can be controlled by a DC applied voltage. The tunability and reconfigurability of electric devices and circuits are a prerequisite for further development of radars, wireless communications, internet, and internet of thinks [1],[2].

Graphene monolayer is a suitable candidate for these applications because of the possibility of electrostatic doping, i.e., the dependence of the carrier density on a gate voltage, and the high mobility of both electrons and holes. As consequence, the electrical conductance and optical constants (dielectric permittivity, refractive index, and losses) can be tuned via gate voltages, inspiring specific devices, such as microwave tunable antennas, reconfigurable transistors, tunable optical modulators, and reconfigurable electrical and optoelectronic circuits [3],[4],[5]. On the other hand, tunability is inherent in ferroelectrics because their electrical permittivity can be changed by an applied DC voltage, many ferroelectric-based tunable devices being fabricated and tested in microwaves and optoelectronics [6],[7].

Besides tunability, graphene monolayers show impressive carrier mobilities, which exceed 200 000 $cm^2/V{\cdot}s$ when the graphene monolayer is suspended in vacuum and the measurements are performed at low temperatures [8]. However, these promising properties are rapidly downgraded when working at ambient conditions and for graphene monolayers transferred on oxide substrates, for instance SiO_2, which limit the mobility in graphene to few thousands $cm^2/V{\cdot}s$ due to extrinsic scattering caused by the morphology, chemistry and structure of the graphene/SiO_2 interface [9]. Large carrier mobility is a prerequisite that cannot be avoided for fast electronic devices, especially for transistors for digital and high-frequency applications. Among more than 200 known 2D materials, graphene monolayers show the highest carrier mobility, accompanied by the most successful growth methods at the wafer scale (4 and 6 inches) [10], raising hopes for ultrafast electronic devices and circuits. Moreover, graphene monolayers are very stable in air, in contrast to the majority of other 2D materials, which require special passivation techniques.

Thus, the challenging issue for ultrafast nanoelectronic devices is to find suitable substrates, with low roughness, on which graphene monolayers can be transferred preserving their high mobility and other physical properties at room temperature, such as ballistic transport over distances longer than 500 nm (graphene on Si/SiO_2) [11] or even 1-10 μm when graphene is encapsulated in h-BN [12]. In this way, a clear pathway could be established to go beyond Moore's law, which is attaining its limits regarding further reduction of transistor sizes due to detrimental short channel effects [13], and to fulfil the Edholm law, which states that the data rates of wired and wireless communications will increase exponentially in the next decade [14]. Both laws are related and call for the design, fabrication and testing of innovative ultrafast devices in the next decade, for which graphene is the best candidate, when transferred on suitable substrates. Why are ferroelectrics the best substrates for graphene monolayers? The state-of-the-art shows that only few applications of graphene-ferroelectric heterostructures as memory devices have been thoroughly investigated (for a review, see [15] and [16]) despite the extraordinary room-temperature mobility, of 70 000 cm^2/Vs, obtained in a graphene monolayer transferred on a PZT substrate epitaxially grown on doped $SrTiO_3$, the latter material acting as back gate [17]. This result is still a record mobility in graphene field-effect transistors (FETs) on substrates, surpassing all other graphene FETs on dielectrics such as Al_2O_3, SiC, SiO_2, Y_2O_3, HfO_2, etc. One reason is that the surface roughness of PZT, as well as of HfO_2-based ferroelectrics, is small, around 0.2-0.5 nm, the other reason being that graphene/ferroelectric heterostructures behave as suspended-like graphene structures due to the reduction of Coulomb scattering on charge impurities at the interface by the built-in field induced by the ferroelectric. We will develop traditional thin-film ferroelectrics, such as PZT, with low roughness, and few-atoms thick HfO_2-based ferroelectrics, with the thickness in the range of 6-9 nm. Further, we will transfer graphene monolayers on these substrates and design, fabricate, and measure innovative nanoscale devices at wafer level. We will

use the PZT substrate as proof-of-concept for nanoscale devices, while all advanced nanoelectronic devices in the project will be fabricated using HfO_2-based ferroelectric substrates at 4-inch wafer scale for an easy integration of graphene devices with CMOS technologies, knowing that HfO_2 is the gate dielectric for the most advanced VLSI circuits containing few billions of transistors [18].

Based on the above concepts, the graphene/ferroelectric heterostructures will allow: (i) the achievement of very high mobilities in graphene-ferroelectric FETs, for high-frequency applications [19], (ii) the fabrication of non-cooled tunable detectors working at high frequencies, (iii) the exploitation of the hysteretic resistance behaviour, essential for neuromorphic applications, such as artificial synapses, where low power is a strong prerequisite, knowing that graphene/ferroelectrics FETs are switched on and off at less than 1-2 V [20], and (iv) the fabrication of reconfigurable microwave circuits and (v) of tunable thermoelectronic devices, since graphene displays a giant thermoelectric effect, which is further enhanced by its high mobility.

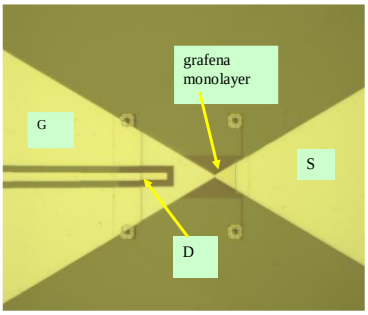
The objectives and/or hypotheses (2018-2022)

The specific objectives of the GRAPHENEFERRO project are:

Objective 1 (2018-2019). Growth of HfO_2-based ferroelectrics, PZT and graphene monolayer transfer at the wafer scale. This is a main objective of the project, dealing with the growth at wafer scale of ferroelectrics and transferring graphene onto them.
Advanced growth methods, such as ALD (atomic layer deposition) and RF magnetron sputtering for HfO_2-based ferroelectrics were developed as well as pulsed laser deposition PLD.

Objective 2 (2019-2020).

1. Graphene field-effect transistors (FETs) based on graphene/ferroelectric heterostructures for high-frequency applications - demo D1.
The graphene/ferroelectric FET is almost "ideal" from the point of view of minimizing the detrimental effects of dielectrics on the graphene channel. Moreover, the high-mobilities make such FETs very appealing for high-frequency applications.
Below (Fig. D1(a)) we present the photos of the first demonstrator – a high frequency detector based on a graphene/ ferroelectric FET in coplanar waveguide technique where the gate and the drain electrodes are formed by a splitting-gate bow tie antenna. The demonstrator was fabricated at the wafer scale, as can be seen from Fig. D1(b).



(a)

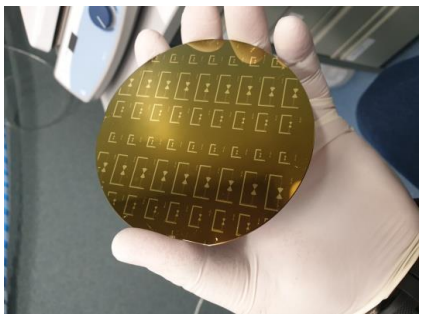

(b)

Fig. D1 Demonstrator D1: (a) detail and (b) at wafer scale

2. The development of a reconfigurable logic circuit based on a graphene/ferroelectric heterostructure - demo 2. We have fabricated and tested a graphene/ferroelectric FET (see Fig. D2) with a graphene monolayer channel grown on a 3-layer deposited stack of 22 nm control HfO_2/5 nm Ge-HfO_2 intermediate layer/8 nm tunnel HfO_2/ *p*-Si substrate. The intermediate layer is ferroelectric and acts as a floating gate. All transistors have two top gates, while the *p*-Si substrate acts as a back gate. These FETs are acting as a two-input reconfigurable logic gates with memory, the type of the logic gate depending only on the values of the applied gate voltages and the choice of a threshold current. In particular, depending only on the values of the gates this transistor is acting as: AND, OR, XOR and NAND gate. Hundreds of FETs were fabricated on the same wafer.

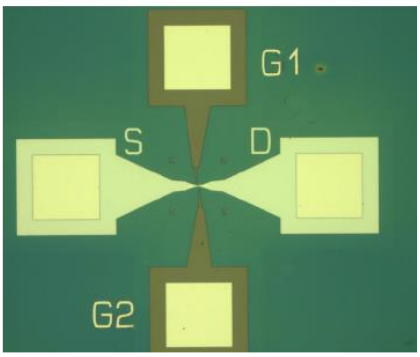


Fig. D2 Demonstrator D2

Objective 3 (2021). Neuromorphic circuits based on graphene/ferroelectric structures – demo 3. We have developed at wafer scale a memtransistor (see Fig. D3) which is the analogue of a brain synapse, showing a switching ratio of 10^7 between on and off states due to the bandgap induced in graphene by the ferroelectric structure and having a memory window of 6 V.

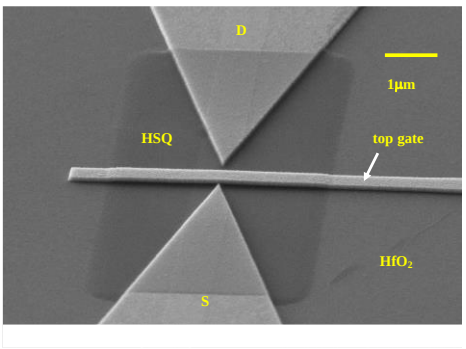
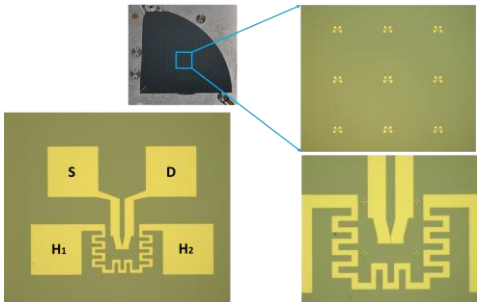
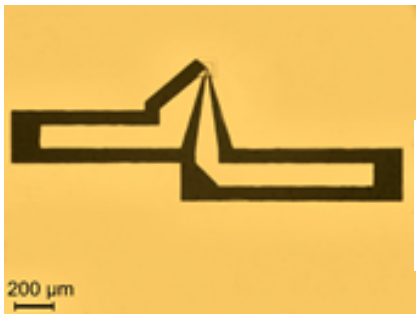


Fig. D3 Demonstrator D3

Objective 4 (2022). Thermoelectric devices based on graphene/ferroelectric heterostructures - demo 4. We have developed at wafer scale two types of thermoelectric devices: graphene/ferroelectric FETs with nonuniform graphene channels, since the channel nonuniformity enhances the thermoelectric performances (Fig. D4(a)), and a microwave thermoelectric FET where the gate is the hot electrode and the source – a massive metallic electrode – the cold electrode (Fig. D4(b)).



(a)



(b)

Fig. D4 Demonstrator D4: (a) graphene/ferroelectric FETs with nonuniform graphene channels and (b) a microwave thermoelectric FET

The project has developed many new nanoelectronic applications of HfO_2-based ferroelectrics and therefore we were invited to present our research results in three review papers [2],[21],[22]. All of them reflect the results obtained in this project.

THE IMPLEMENTATION OF THE OBJECTIVES AND RESULTS

1. Implementation of objective 1 (2018-2019)

The goals of objective 1 are the growth at waferscale of HfO_2-based ferroelectrics and PZT. This objective had three tasks:

1.1 The growth and characterization of HfO_2-based ferroelectrics using atomic layer deposition (ALD) by CO

1.2 The growth of HfO_2-based ferroelectrics using magnetron sputtering (MS) by P2

1.3 The growth of PZT at the wafer level by P3

1.4 The atomistic simulation of the graphene/ferroelectric interface by P1.

Implementation of task 1.1: The growth and characterization of HfO_2-based ferroelectrics using atomic layer deposition (ALD)

The HfO_2-based ferroelectrics were grown successfully by ALD methods. Two growth modes were applied: laminated and mixed by doping HfO_2 with Zr (HfZrO) and Al (HfAlO) on 4-inch Si wafers. The two modes are described as: (i) mixed mode, where the two ALD precursors were mixed in variable proportions (1:1, 2:1, 20:1) and then oxidated, (ii) laminated – the ALD cycles are alternated in a proportion of 4:1 of HfO_2 and ZrO_2 (for HfZrO) or Al_2O_3 for (HfAlO). The laminate mode was finally selected since initial measurements have shown that the roughness of the deposited material is smaller than in the mixed mode.

Thus, the nominally 6-nm-thick $Hf_xZr_{1-x}O_2$ films were grown at 250 °C on high-resistivity Si (100) substrates by Atomic Layer Deposition (ALD) using a Cambridge NanoTech F200 ALD reactor. The ALD precursors were Tetrakis (ethylmethylamido)hafnium (TEMAHf), Tetrakis (ethylmethylamido)zirconium (TEMAZr) and water. Growth was performed in a laminate ALD mode using 30 super-cycles of TEMAZr-H_2O-TEMAHf-H_2O, all separated by argon purges. The resulted ferroelectric is termed further as HfZrO

Several structural measurements were performed:

- **The film thickness** was confirmed by spectroscopic ellipsometry (Woollam M2000) to be 5.6±0.2 nm using a four-layer optical model: air/$Hf_xZr_{1-x}O_2$/SiO_2/Si
- **The composition** of the nominally $Hf_xZr_{1-x}O_2$ films was investigated by X-ray photoelectron spectroscopy (XPS) using a Kratos AXIS ULTRA spectrometer with a source of monochromatic Al K_α of 1486.58 eV. The nominally $HfZrO_4$ films are clearly non stoichiometric ($Hf_{0.45}Zr_{0.55}O_{1.76}$),
- **The orthorhombic phase** specific to HfO2-ferroelectris was searched using the grazing incidence X-ray diffraction (GIXRD) pattern of the $Hf_{0.45}Zr_{0.55}O_{1.76}$ film and was measured on a Rigaku Smartlab system using the Cu K_α line at an angle of incidence of 0.35°. The orthorhombic phase with the Pbc21 symmetry was identified in the GIXRD spectrum.
- **The roughness** measured by AFM was identified to be 0.177 nm when HfO_2 was doped with Zr and 0.2 nm when HfO_2 was doped with Al, both materials being ferroelectrics.

Results beyond the state of the art for HfZrO grown on Si: the explanation of ferroelectricity in HfZrO grown directly on Si or Si/SiO_2 is the occurrence of a novel ferroelectric paracrystalline phase by oxygen vacancies engineering during the ALD growth directly on Si. This particular paracrystalline phase is defined as having short- and medium-range ordering in its lattice, but lacking crystal-like long-range ordering, and is assumed to be formed by the interplay of a **new rhombohedral polar R3m ferroelectric phase** (evidenced typically at 30.5° in GIXRD measurements) with a minority orthorhombic $Pca2_1$ phase (see Fig. 1.1). See: M. Dragoman, M. Aldrigo, D. Dragoman, S. Iordanescu, A. Dinescu, M. Modreanu, HfO_2-based ferroelectrics applications in nanoelectronics, Physica Status Solidi Rapid Res. Lett., https://doi.org/10.1002/pssr.202000521, 2021.

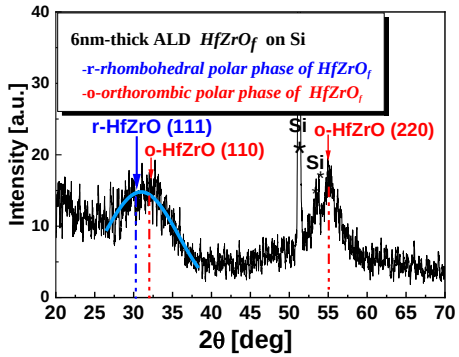


Fig. 1.1 GIXRD pattern for the HfZrO thin film on Si (100) indicating the rhombohedral phase

Electrical measurements were performed to test the validity of our results.

The **PFM** (piezo-force microscopy) analysis of HfZrO deposited on a doped Si/SiO_2 wafer in the same conditions as above was performed before graphene transfer because of the need of using doped Si as a bottom electrode for PFM analysis (the upper electrode is a metal-coated AFM tip). Further, the samples were fixed on stainless steel holders with silver paste for a good electric contact. PFM images were recorded using a commercial atomic force microscope equipped with a lock-in amplifier (SR830, Stanford Research System). An AC modulation voltage was applied to a metal-coated tip (NSC36 TiPt – Mikromasch; cantilever A with nominal force constant ~1 N/m) from the external lock-in amplifier, which demodulates the AC component induced in the PSPD deflection signal. The spontaneous polarization direction is indicated by the phase difference between the tip vibration signal and the AC modulation voltage, while the longitudinal piezoelectric coefficient is proportional to the tip vibration amplitude. For the local manipulation of ferroelectric domains ("writing") the tip was held at 0 V, whereas a DC bias between -10 V and 10 V was applied to the bottom electrode during scanning. The local mechanical response was determined ("read") by applying an AC bias to the tip while the bottom electrode was held at 0 V. In order to investigate the domain-switching behaviour, several writing/reading scan sets were performed, as follows: initially, the positive bias was applied to the bottom electrode during a 5 µm×5 µm scan; next, the negative bias was applied during a 2 µm×2 µm scan taken in the middle of the previous area; finally, the response was recorded over a 10 µm×10 µm area centred on the first two. Figure 1.2 shows the PFM amplitude and phase images of the zirconium-doped HfO_2 thin films. The amplitude image represents the strength of polarization (intensity of the local mechanical response) and the phase image indicates the direction of polarization (phase shift between the excitation and the response). It can be seen that the local response differs between the initial and the written areas. Also, the pristine material has a non-zero response, with a phase shift similar to the 2 µm×2 µm area, where the bottom electrode was held at a negative bias. In the PFM amplitude images, the bright regions indicate domains with strong out-of-plane polarization, oriented either up or down. Dark regions are observed at the domain boundaries, where the out-of-plane polarization disappears. In the PFM phase images, the bright regions correspond to domains with upward polarization and the dark regions represent domains with downward polarization. The phase shift differs by 180° between successively written areas. Figure 1 demonstrates that zirconium-doped HfO_2 thin films show an easy switching of polarization along the poling direction, with clear boundaries between upward and downward domains observed in phase and amplitude images.

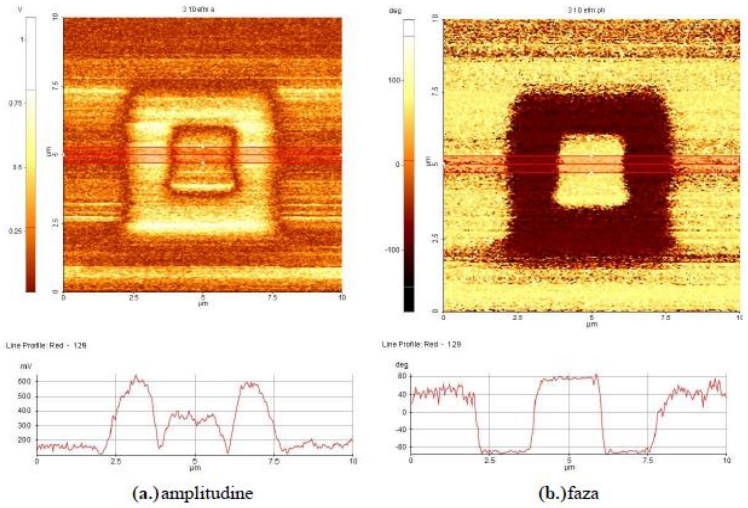


Fig. 1.2 PFM for $HfZrO_2$ (mixed 1:1)

Write on 5 µm × 5 µm, 5V ; write pe 2 µm × 2 µm, -10V ; read on 10 µm × 10 µm, 3V AC

The polarization dependence P(E) with the applied DC field was measured using the Sawyer-Tower method consisting of a digital oscilloscope (Wavesurfer 3024 - Teledyne LeCroy) and a pulse generator (NI PXIe-1078 - National Instruments). The results are: the remanent polarization P_r= 22 µC/cm² and the coercive field is 0.7 MV/cm.

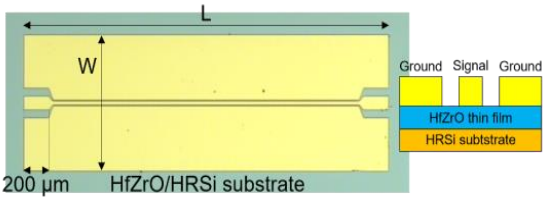
Results beyond the state of the art:

1. We have fabricated HfZrO capacitors to test the ferroelectricity of HfO_2 doped with Al, which have shown not only excellent ferroelectric properties but excellent non-volatile memory performances. The results are published in:

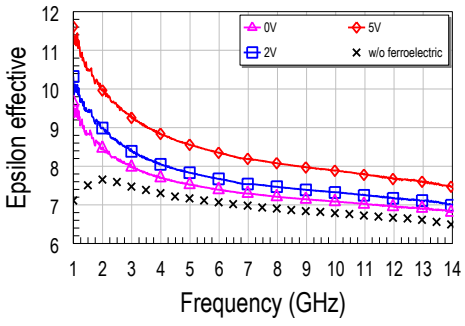
S. Vulpe, F. Nastase, M. Dragoman, A. Dinescu, C. Romanitan, S. Iftimie, A. Moldovan, N. Apostol, Physical properties of the ferroelectric capacitors based onAl-doped HfO_2 grown via Atomic Layer Deposition on Si, Applied Surface Science 483, 324-333 (2019), 10.1016/j.apsusc.2019.03.166

2. For the first time we have measured the HfO_2-based ferroelectrics in microwave to test the dependence of the electrical permittivity on the applied DC bias – a property specific only to ferroelectrics

In this respect, special coplanar waveguides (CPW) having two different lengths were deposited using e-beam metallization: 50 nm/500 nm thick Ti/Au layer. The width of the CPW is 1 mm, whereas the lengths are L_A =6.671 mm and L_B = 2.393 mm (see Fig. 1.3(a)). The dependence of the electrical permittivity on the applied field is represented in Fig. 1.3(b).



(a)



(b)

Fig. 1.3 Measurement of HfZrO in microwaves: (a) CPW, (b) permittivity of HfZrO in microwaves at different DC applied voltage.

Why this result is so important?

The electrical permittivity dependence on the DC applied voltage was used for tunable microwave phase shifters and other tunable microwave devices, but it was abandoned since the required DC voltage for 60° shifts was in the range 50-100 V in the case of PZT and perovskite ferroelectrics. In our case, we need only 2 V to produce the same phase shift. Therefore, phased antenna arrays to be used in 5G and 6G communications can be biased by a battery (see: M. Dragoman, M. Modreanu, I. Povey, S. Iordanescu, M. Aldrigo, A. Dinescu, D. Vasilache, C. Romanitan, 2.55 GHz miniaturised phased antenna array based on 7 nm-thick HfxZr1−xO2 ferroelectrics, Electronics Letters 54, 469-470 (2018). **In this way, the task 1.1 was successfully accomplished (see Fig. 1.4). The HfZrO deposition at the wafer level is performed, is reproducible, and in several ways the results are beyond the state of the art.**

Fig. 1.4 HfZrO wafers grown by ALD on 4 inch Si wafers

Implementation of task 1.2: HfO_2-based ferroelectrics using magnetron sputtering

Growth method description: Ferroelectric HfO_2 films were prepared by magnetron sputtering deposition (Gamma 1000 C sputtering equipment, Surrey NanoSystems) and subsequent rapid thermal annealing (RTA in AS Micro rapid thermal processor, Annealsys). The HfO_2 film consists of a stack of 3 layers of 22 nm control HfO_2/ 5 nm Ge-HfO_2 intermediate layer/ 8 nm tunnel HfO_2/ *p*-Si substrate (7 – 14 Ωcm). The two HfO_2 layers in the stack were deposited by RF power of 40 W, while the Ge-HfO_2 alloy in the intermediate layer was obtained by co-deposition of Ge and HfO_2 (in a volume ratio Ge:HfO_2 of 55:45) using 10 W DC and 40 W RF powers, respectively (more details are found in the paper written by some authors of the project: Nanotechnology 28, 175707 (2017)). This trilayer structure was annealed by RTA at 600-620 °C for formation of ferroelectric HfO_2.

Several structural and electrical characterizations were needed to validate the ferroelectricity

-Structural characterization: the formation of HfO_2 orthorhombic/tetragonal phase was studied by HR-TEM microscopy by the lattice fringe of 0.295 nm in the intermediate Ge-HfO_2 layer and the formation of HfO_2 monoclinic phase with 0.367 nm lattice fringe for the (011) plane in the control and tunnel layers. In the intermediate layer, Ge strains the HfO_2 lattice due to the formation of 2-3 nm Ge quantum dots (QDs) with hexagonal structure grown topotactically on the HfO_2 orthorhombic structure positioned at the HfO_2 boundaries. The results are presented in Fig. 1.5.

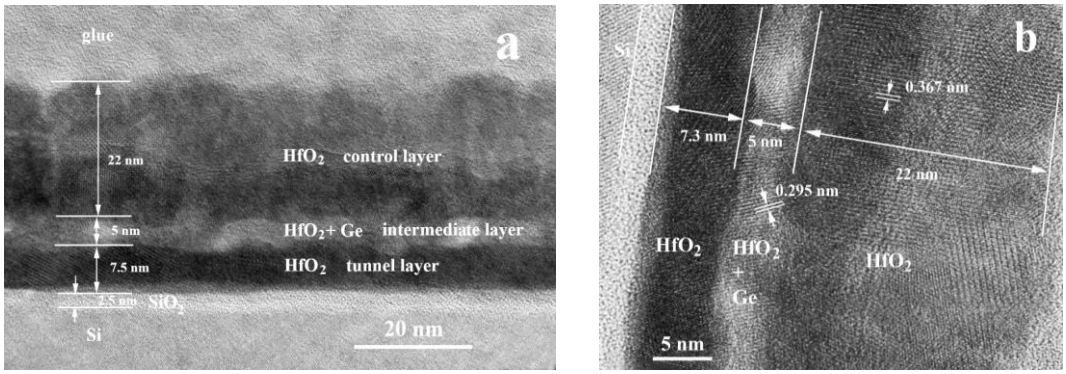


Fig. 1.5 XTEM images of the control HfO_2/HfO_2+Ge intermediate layer/tunnel HfO_2/Si substrate structure. The XTEM specimen is prepared after the annealing of the 3-layers-stack, but before graphene deposition. a) Low magnification image, and b) High resolution image showing the presence of the orthorhombic/tetragonal HfO_2 phase (0.295 nm lattice fringe) in the intermediate layer and the monoclinic HfO_2 phase (0.367 nm for (011) plane) in the control and tunnel layers

-Electrical measurements: as in task 1.1, PFM, capacitance and polarization dependence on applied voltage measurements were performed. Here we illustrate our results with capacitance-voltage measurements.

***C–V* hysteresis** loops measured at 1 MHz for different biasing times at +4 V and –4 V are presented in Fig. 1.6. All *C–V* hysteretic characteristics are counterclockwise. By measuring four consecutive cycles for a biasing time of 5 min, we observed very small differences between *C–V* loops. One can see that the memory window increases from 2.4 to 5 V when the biasing time increases from 1 to 10 min. The high value of 5 V for the memory window shows the contribution of ferroelectric HfO_2 besides that of Ge QDs charge storage centres (Fig. 1.6).

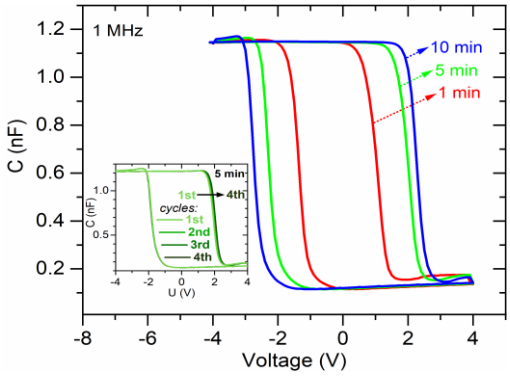


Fig. 1.6 C – V hysteresis loops measured at 1 MHz for different biasing times at +4 V and –4 V. Insert: Four consecutive C – V cycles measured for 5 min biasing time

The P(E) measurements have shown similar results in terms of the remanent polarization and coercive fields as in the case of the ALD method. So, the second growth method for HfO_2-based ferroelectrics has demonstrated that HfO_2-based ferroelectrics can be grown in a reproducible manner at the wafer scale.

Results beyond the state of the art: The HfGeO ferroelectric is a new ferroelectric and this material has allowed us to obtain for the first time ferroelectric memtransistors fabricated at the wafer scale with low drain and gate voltages to be used in the project in the following stages, in 2021-2022 (see M. Dragoman, A. Dinescu, F. Nastase, D. Dragoman, Memtransistors based on nanopatterned graphene ferroelectric field-effect transistors, Nanomaterials 10, 1404 (2020)).

Implementation of task 1.3: The growth of PZT at the wafer level

Motivation: At the time when we have written this project (summer of 2016, but the project has started in the summer of 2018!) PZT (Lead zirconate titanate) **was the only ferroelectric which could be used for the goals of the project. HfO_2-based ferroelectrics were grown only by two teams in the world (Germany and Japan) and since the project has asked an assumed high risk for the implementation, PZT was selected as a backup solution in the case that no growth method for HfO_2-based ferroelectrics will be successful. Now, we see that it was not the case. However, we wanted to have PZT grown at the wafer level and grown on Si. These targets are beyond the state of the art in the case of PZT and the results are presented below for a PLD installation able to growth 10 cm PZT wafer directly on Si/SiO_2.**

Structural characterization: the layers are highly adherent to the substrate, are textured (see XRD spectra-Fig. 1.7(a), have a controlled morphology (see SEM image-Fig. 1.7(b)), and exhibits ferroelectric properties (see AFM/PFM images-Fig. 1.8), being thus fully compatible with graphene deposition.

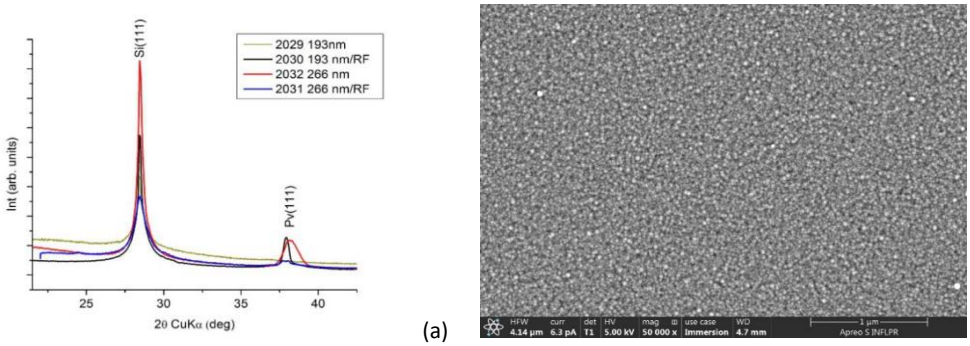


Fig. 1.7 The XRD of PZT/Si wafer (b) SEM image of the PZT

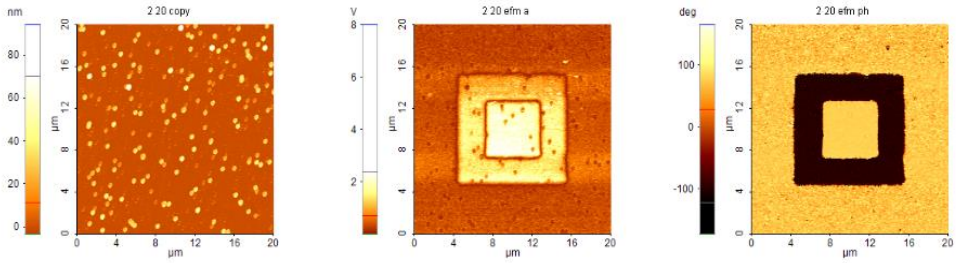


Fig. 1.8 PFM of PZT / Si wafer.

Electrical measurements: PFM measurements (Fig. 1.8) were performed to verify ferroelectricity of the PZT/Si wafer. The measurements were made on the same equipment as for the other two methods above and the description of the method is found in task 1.1 and will be not repeated here. The phase shift differs by 180° between successively written areas. The PLD equipment able to grow the PZT/Si wafer is shown in Fig. 1.9.

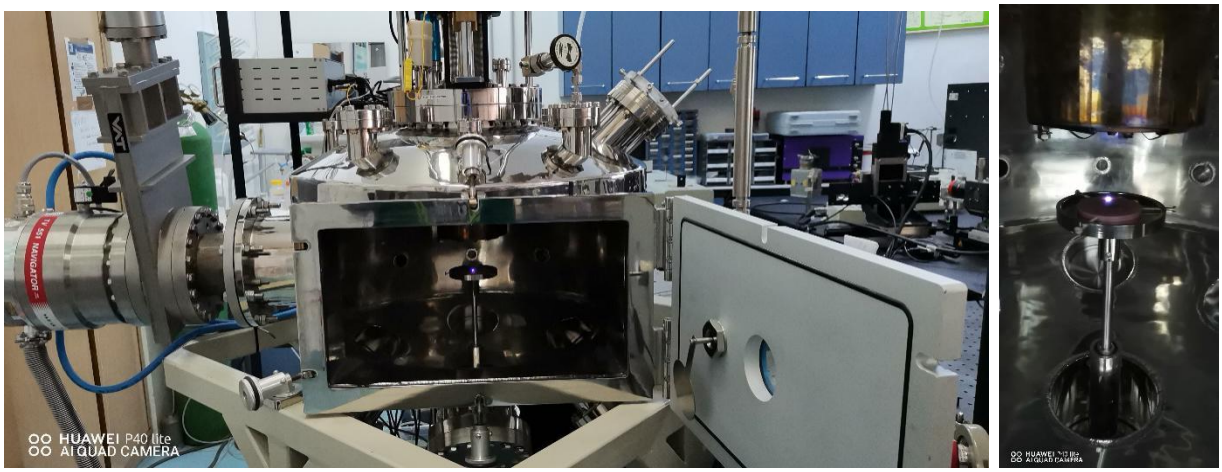
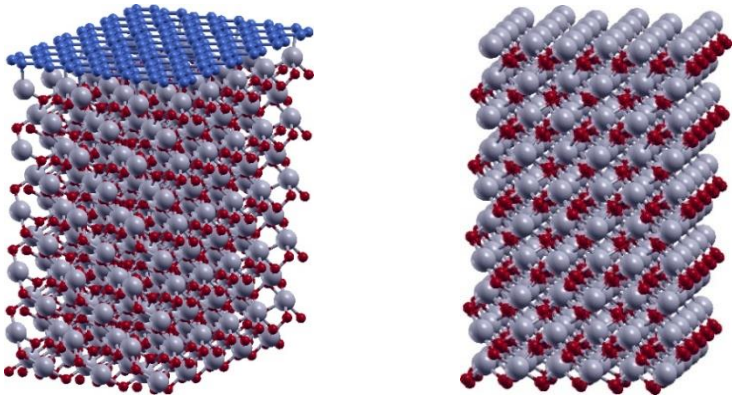


Fig. 1.9 The PLD equipment able to grow 10 cm PZT/Si wafers implemented at INFLPR –Magurele.

Implementation of task 1.4: Atomistic simulations of the graphene/ferroelectric heterostructure

This is an important task targeting the next objective of the project. Two structures were studied: graphene/HfO_2 terminated with O or Hf atoms (see Fig. 1.10). The DFT SIESTA sofware package was used for simulations.



Oxygen terminated (red spheres) Hf terminated (grey spheres)

Fig. 1.10 Graphene/HfO_2 structures modelled with SIESTA

The atomistic simulations are presented below:

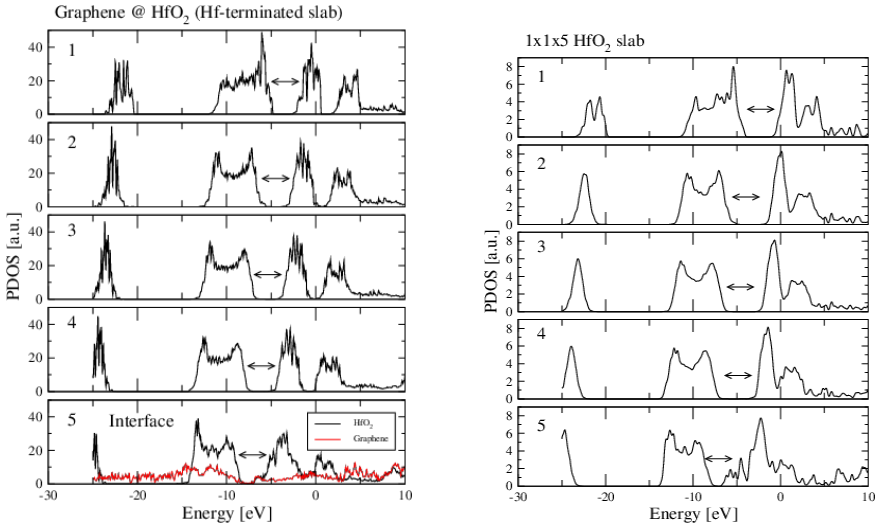


Fig. 1.11 DOS of the two structures in Fig. 1.11

Progress beyond the state of the art: these simulations (see Fig. 1.11) have indicated for the first time that ferroelectric HfO_2 could induce a band gap of 0.3 eV in graphene, a crucial issue for using graphene in digital applications and high frequencies, result which was never reported previously in the literature (see: G. A. Nemnes, D. Dragoman, M. Dragoman, Graphene bandgap induced by ferroelectric Pca21 HfO2 substrate: a first-principles study Phys. Chem. Chem. Phys. 21, 15001-15006 (2019)).

CONCLUSIONS FOR OBJECTIVE 1

The objective 1 had four tasks:

1. 1 The growth and characterization of HfO_2-based ferroelectrics using atomic layer deposition (ALD)
1.2 The growth of HfO_2-based ferroelectrics using magnetron sputtering (MS)
1.3. The growth of PZT at the wafer level
1.4 The atomistic simulation of the graphene/ferroelectric interface

Each of them was accomplished and finished. We have described the growth methods, the structural characterizations, electrical characterizations and finally the simulations of graphene /ferroelectric heterostructures.

What have we achieved?

-the growth at the wafer level of three ferroelectrics with reproducible results, all being CMOS compatible, and of the PZT in post-CMOS processes. The parameters of the ferroelectrics are at the level of the state of the art.

-results beyond the state of the art were explained for each task, all being published in Q1 and Q2 journals which publish ONLY results beyond of the state of the art, and presented at international conferences

-the teams have worked very well together, a protocol of measurements was created, such that a material already fabricated should be characterized with the same methods and whenever possible on the same equipment, assuring in this way the validity and reproducibility of our results. We have used several runs of fabrications and many measurements (here are presented less than 20% of them!!!).

2. Implementation of objective 2 (2019-2020): Graphene field-effect transistors (FETs) based on graphene/ferroelectric heterostructures for high-frequency applications-demo D1.

The goals of the objective are: the design, fabrication and measurements of graphene/ferroelectric transistors showing high mobility and trans-conductance for high frequency applications, i.e., a high-frequency detector which must be reproducible –which is the first demo D1 of the project.

This objective has three tasks:

2.1 The design of a FET integrated with antenna arms

2.2 The fabrication of an integrated FET with antenna arms at the wafer level

2.3 Measurements at the wafer level in DC and microwaves and THz.

2.1 Implementation of the task 2.1: The design of a FET integrated with antenna arms

The first integrated circuit based on active device – a graphene FET, integrated with an antenna on HfZrO is presented in Fig. 2.1 while in Fig. 2.2 the optical image of the demonstrator is shown. The entire circuit is a microwave detector, where the gate (G) and source (S) electrodes of a FET transistor are forming the arm of a split bow-tie antenna, while its drain electrode is the output of the detector. The graphene monolayer is the channel of the transistor. Coplanar lines (CPW) are used to bias the drain and gate electrodes while the source is grounded by CPW. The CPW is formed from three electrodes, the central electrode is the signal electrode while the outer electrodes are grounded by probe tips applied for high frequency excitation. The demonstrator was first designed and simulated on a 3D electromagnetic simulator (CST) and the design is presented below (Fig. 2.1). The demonstrator D1 is a field effect transistor (FET) having as channel a graphene monolayer transferred on HfZrO (6nm)/Al_2O_3 (20nm)/HR Si substrate.

The relations between various frequencies and the dimensions of the detector resulted from simulations are presented below, where the significance of L and W result from Fig. 2.1 while λ_g is the wavelength in HfZrO and was established using the measurements performed in task 1.1.

Frequency	λ_g	L	W
24 GHz	4,62 mm	14,5 mm	~10 mm
38 GHz	2,61 mm	8,7 mm	8,42 mm
60 GHz	1,76 mm	5 mm	4,64 mm

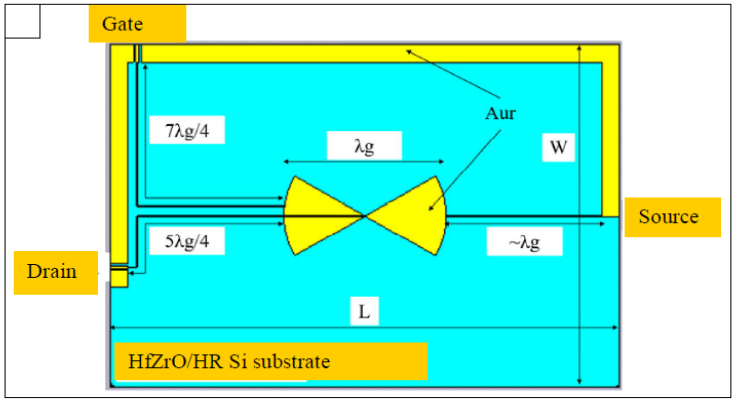


Fig. 2.1 The layout for the simulation of demonstrator D1 HfZrO/Al2O3/HR Si

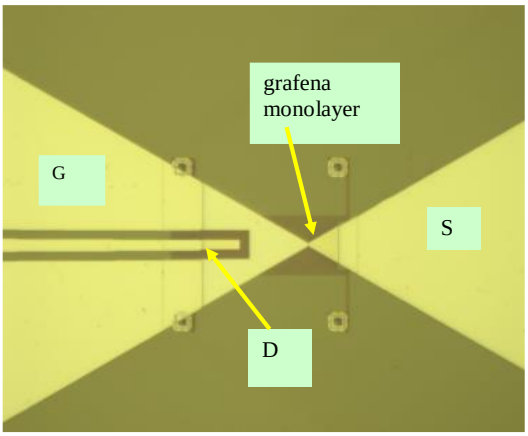


Fig. 2.2 The optical image of the demonstrator

The simulations of the splitting-gate bowtie antenna regarding the reflection losses and gain were obtained first at 24 GHz, 38 GHz and 60 GHz. The gain of antennas is very good in the range -45° and 45° and is 7.16 dB at 24 GHz, 11.23 dB at 38 GHz and 6.26 dB at 60 GHz. The radiation efficiency is high: 91.6% at 24 GHz, 90.4% at 38 GHz and 83.95% at 60 GHz and is depicted in Fig. 2.3. The reflection coefficients |S11| are also very good: -7.48 dB at 24 GHz (Fig. 2.3 (a)), -12.7 dB at 38 GHz (Fig. 2.3 (c)) and -20.78 dB at 60 GHz (Fig. 2.3 (e)).

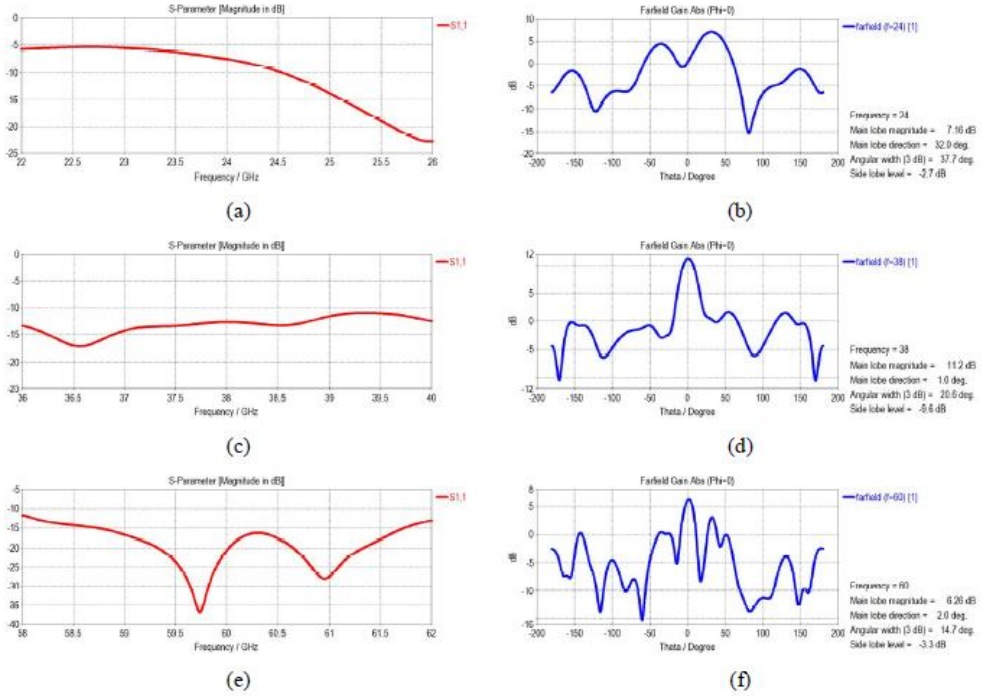


Fig. 2.3 The simulations of the bow-tie antenna

Implementation of task 2.2: The fabrication of an integrated FET with antenna arms at the wafer level

The implementation of this task is rather complex and requires several steps.

Step 1. HfZrO was grown according to the growth methods described in Objective 1 having a 6 nm thickness. Structural and electrical characterizations were performed to test the ferroelectricity and the quality of growth methods, as described in Objective 1. The HfO_2 ferroelectrics were placed on an Al_2O_3 layer (20 nm) which isolates the charges of the high-resistivity Si (> 10 kΩ/square) used especially because it **has low losses at high frequencies up to THz range.**

Step 2. The graphene was transferred on the HfZrO (6 nm)/Al_2O_3 (20 nm)/HR Si substrate. The graphene was transferred at the wafer level of 4 inches and 6 inches by Graphenea with our help, and when small areas of less than 2 inches were required, we have used electrochemical transfer using our in-house installation (Fig. 2.4)

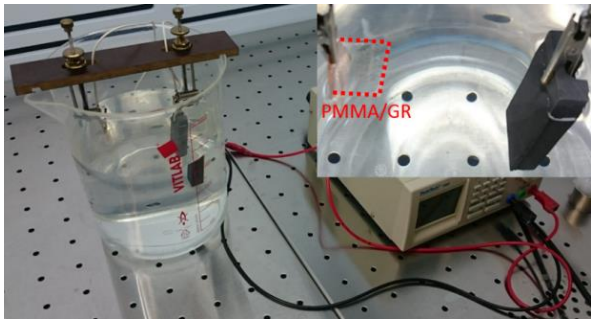


Fig. 2.4 Graphene transferred electrochemically at IMT Bucharest

Raman spectroscopy was used to characterize the graphene deposition on HfZrO ferroelectrics. We have obtained the following results:

Graphenea (Spain) graphene transfer on HfZrO:

Probes	FWHM(G)	FWHM(2D)	I_D/I_G	I_{2D}/I_G
14_13	30.22	33.48	3.52	2.81
15_08_0_0 s1	22	32.22	0.65	1.01
15_08_0_1 s2	17.11	37.77	1.53	3.56
15_08_1_0 s3	11.78	35.77	0.53	4.56
15_08_1_1 s4	27.11	33.77	4.29	2.42

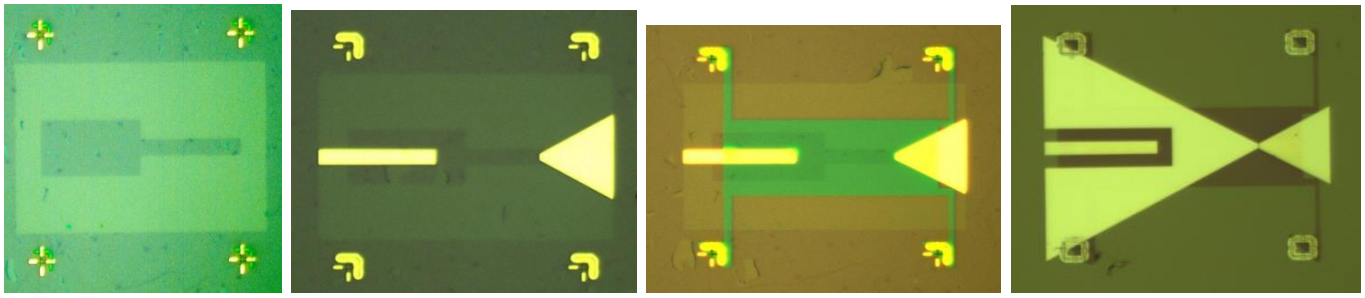
IMT method of graphene transfer on HfZrO:

Sample	FWHM(G)	FWHM(2D)	I_D/I_G	I_{2D}/I_G
15_30	14	33.55	1.24	3.05
15_42	18.44	36.88	4.85	2.23
16_28_0_0	14.89	36	0.64	2.9
16_28_0_1 s2	12.67	36	0.43	2.48
16_28_1_1 s4	13.33	32.66	1.12	2.91

We see that the report I_{2D}/I_G is higher than 2 in all cases, meaning that the graphene monolayer is transferred with few defects in the case of Graphenea and more defects in the case of IMT, but the density of defects depends on the CVD grown conditions, which are different in the two situations.

Step 3. The fabrication of an integrated FET with antenna arms at the wafer level.

The first step consists in graphene channel patterning by e-beam lithography and reactive ion etching (RIE). The wafer was spin coated with PMMA 950k A4 with a thickness of 250 nm, exposed in an e-beam lithography equipment (Raith e_Line) at 30 kV and 100 pA beam current, and then developed for 1 min in a mixture of MIBK:IPA (1:3). In order to etch the graphene layer, the wafer was exposed to oxygen plasma for three seconds in a RIE equipment (SENTECH Instruments- SI 220). The remaining PMMA covering the graphene channel was removed in acetone. The second fabrication step consists in source (S) and drain (D) patterning, metallization, and lift-off. In this respect, the substrate was covered by spin coating with a layer of PMMA 950k A2 with a thickness of 100 nm, exposed in an e-beam lithography equipment (Raith e_Line) at 10 kV and 35 pA beam current, then developed for 30 sec in a mixture of MIBK:IPA (1:3) and subsequently deposited with Ti/Au (5/35 nm) in a highly directional e-beam evaporation equipment (TEMESCAL FC2000). For lift-off, the sample was placed in acetone for few hours and, then sonicated in IPA for 30 sec. The wafer was spin coated with a 40-nm-thick HSQ (hydrogen silsesquioxane) layer, a negative electroresist used in microelectronic industry with very good insulating properties. Afterwards, it was patterned by e-beam lithography (30 kV, 100 pA, 1000 μC/cm2) and developed for 70 sec in a solution of tetramethylammonium hydroxide (TMAH) 2.6%, in DI water. The last step is the fabrication of contacts by patterning, metallization and lift-off. The substrate was spin coated with a PMMA 950k A4 layer with a thickness of 350 nm, exposed in an e-beam lithography equipment (Raith e_Line) at 10 kV and 500 pA beam current, then developed for 120 sec in a mixture of MIBK:IPA (1:3). Subsequently, it was deposited with Ti/Au (5/145 nm) in a highly directional e-beam evaporation equipment (TEMESCAL FC2000). For lift-off, the sample was placed in acetone for few hours, then sonicated in IPA for 30 sec. We present in Fig. 2.5 several images taken during the fabrication process. The FET channel has a length of 200 nm and a width of 3 μm.



(a) (b) (c) (d)

Fig. 2.5 Optical images of demo fabrication steps: (a) e-beam patterned graphene channel, (b) drain and source metallic deposition, (c) 40 nm HSQ gate dielectric deposition, (d) metallic gate deposition

Some of the graphene channels were patterned with nanoholes having 20 nm diameter and a period of 100 nm (Fig. 2.6). The reason is that HfZrO induces a bandgap in graphene of 0.2 eV (see M. Dragoman et al., Graphene bandgap induced by ferroelectric HfO_2 doped with Zr (HfZrO), Nanotechnology 31, 275202 (2020)), which is the experimental confirmation of the simulations done previously by P1, but additionally the holes are introducing also a bandgap enlarging the bandgap up to 0.4 eV, which is compatible with digital applications.

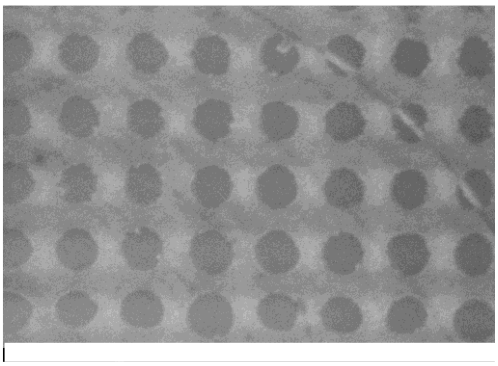


Fig. 2.6 The nanopatterned graphene channel

Step 4. DC and microwave measurements. The drain-current (I_D) versus drain voltage (V_D) dependences at various gate voltages (V_G) and I_D versus V_G at various V_D voltages are presented below. We observe in the I_D -V_D dependence (Fig. 2.7) that the transistor has an on current of about 1 mA and is turned off at a gate voltage of -2 V, which is an amazing result since the graphene monolayer is not a semiconductor, has no bandgap and thus no off state. As we will see, this is a leap towards digital applications of graphene. On the other hand, the I_D –V_G dependence (Fig. 2.8) is typical for a ferroelectric transistor, i.e., a hysteretic behaviour indicating the memory effect. From the dependence

$$I_{D,on}/I_{D,off} \propto \exp(E_g/k_BT)$$

we extract the bandgap of 0.3-0.4 eV, while the mobility of carriers is 8 900 cm^2/Vs.

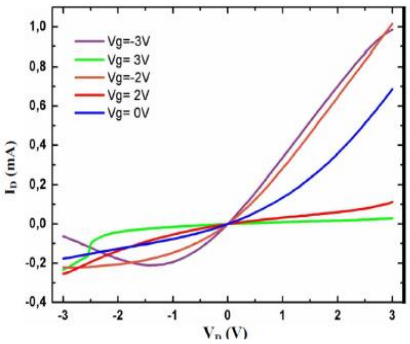


Fig. 2.7 I_D –V_D dependence

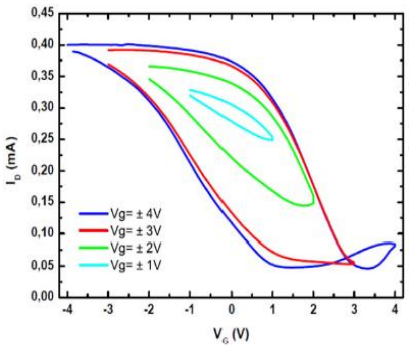


Fig. 2.8 I_D –V_G dependence

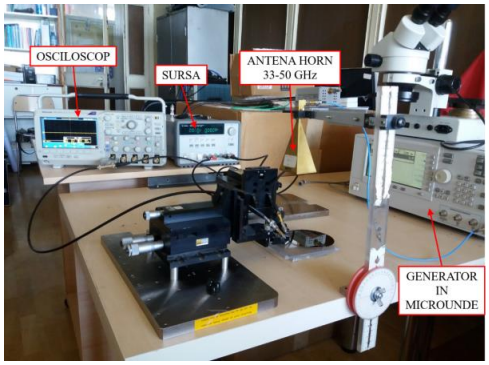


Fig. 2.9 Setup to measure the demonstrator in microwaves

The setup to measure the demonstrator in microwaves is displayed in Fig. 2.9. The first measurements with a tunable microwave generator modulated the signal with 1 kHz rectangular pulses. All measurements are performed at room temperature. We have obtained the following results:

Frequency	V_G	V_D	DC voltage detected
4 GHz	0 V	+0.02 V	12 mV
4 GHz	0 V	-0.02 V	7.2 mV
4 GHz	+2 V	+1.02 V	11.4 mV
4 GHz	-2 V	-1.02 V	11 mV
6 GHz	+2 V	+1.02 V	1.04 mV
12 GHz	+2 V	+1.02 V	0.88 mV

The waveforms of the above detected signals are presented in Fig. 2.10

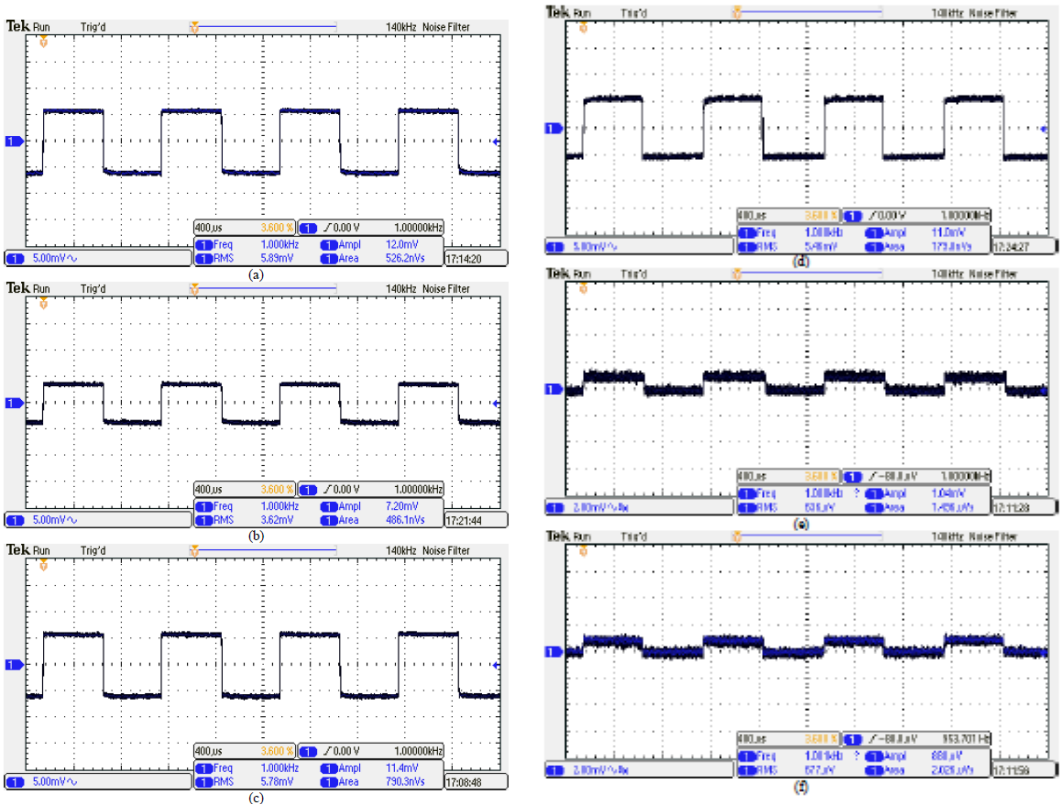


Fig. 2.10 The detected waveforms in the range 4-12 GHz

Terahertz measurements. Since the mobility of graphene/HfZrO FET is very high, higher than of typical semiconductors such as Si, GaN, GaAS and similar to InP, which is the semiconductor material used for realization of transistors at 1 THz, we have measured the graphene/HfZrO in the THz domain using the equipment TeraView PS3000 in transmission mode. The spectral resolution is 1 cm^{-1} and 1800 data points were collected automatically by the setup. Since THz measurements are very sensitive to water vapors the wafer was cleaned by N_2. The result is displayed in Figs. 2. 11. and 2.12.

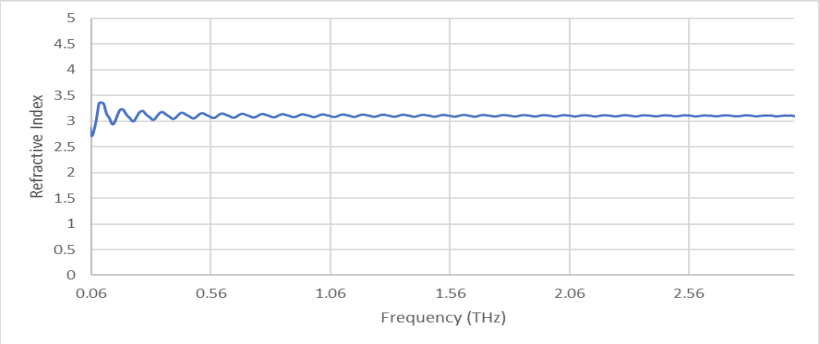


Fig. 2.11 The refractive index of graphene/HfZrO up to 3 THz.

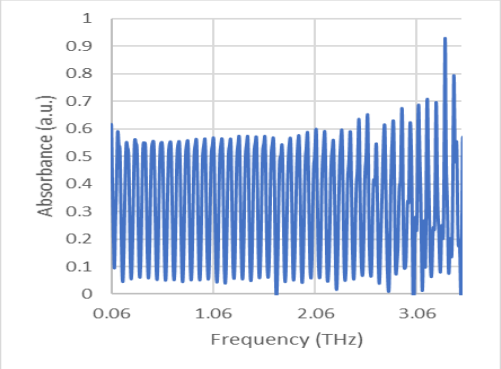


Fig. 2.12 The absorbance of graphene/HfZrO up to 3 THz.

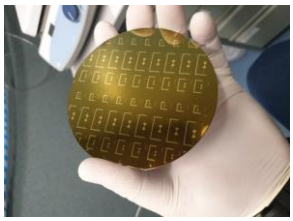
We see that the index of refraction is almost constant and the absorption is very low up to 3 THz. This means that we can scale down the graphene/HfZrO FET dimensions up to 3 THz and the D1 will work.

Conclusions for the objective 2

The goals of the objective 2 were accomplished at the end of 2020. The design, fabrication and measurements of the graphene/HfZrO FET were performed up to 3 THz. The demo 1 has very good performances.

Results beyond the state of the art in Objective 2:

-demo 1 is the first integrated circuit based on graphene/ferroelectrics working in microwaves and produced at the wafer level. See the optical image of demo 1 below:



M. Dragoman, M. Aldrigo, D. Dragoman, S. Iordanescu, A. Dinescu, M. Modreanu**,** The rise of ferroelectricity at nanoscale, *Nanotechnology Magazine*, vol. 15, pp. 8-19 (2021).

-the experimental evidence of a bandgap induced in graphene mononolayer by HfO_2-based ferroelctrics (see M. Dragoman, A. Dinescu, F. Nastase, A. Moldovan, D. Dragoman, Graphene bandgap induced by ferroelectric HfO_2 doped with Zr (HfZrO), Nanotechnology 31, 275202 (2020)). It is well known that graphene monolayers have no bandgap and this fact implies that graphene FETs have no OFF state, which means that they cannot be used in digital applications or in nonlinear applications such as detection at high frequencies. We have solved this longstanding conundrum.

-**the very high mobility of the FET**, i.e., 9 000 cm^2/Vs makes this transistor to work up to the THz region, and is higher than the mobility of Si, GaAs, GaN semiconductor and similar to that of InP.

-**first THz measurements on graphene/HfZrO FETs**.

-**all measurements were performed on all graphene/HfZrO FETs and 70% of the measured results were reproducible**.

Implementation of the Objective 3 (2021): Neuromorphic circuits based on graphene/ferroelectric heterostructures (this objective encompasses the demo 2 of objective 2 and demo 3 of objective 3)

Objective 3 consists from two distinct demonstrators, which reflect the main research directions of neuromorphic computation. First, we will present a reconfigurable logic gate based on graphene/HfGeO ferroelectric, which is the demo 2 of objective 2. This reconfigurable logic gate has an inherent memory due to the ferroelectric and thus the logic and memorization operations are made in the same place, in deep contrast with normal computers where logic operations and memorization are made separately in two distinct units, i.e., ALU and Memory. This device is thus in the same trend with in-memory neuromorphic computing, where there is no separation between memory and logic devices and in this way a lot of energy is saved. The second demonstrator – the demo 3 – is a memtransistor, which is an electronic analogue of a neuronal synapse. We have fabricated an array of 225 transistors on the same wafer to form a cross-bar array. Thus, the tasks of this objective are:

3.1 The growth of the HfO2-based ferroelectric.

3.2 The reconfigurable in-memory logic gate based on the graphene/ferroelectric heterostructure-demo2

3.3 The memtransistor-an electronic analogue of a neuronal synapse.

Implementation of the task 3.1: The growth of the HfO2-based ferroelectric

We have grown the HfZrO using ALD, HfGeO using magnetron sputtering, and PZT via PLD, but the best results were obtained for the HfGeO ferroelectrics. Since the growth methods were well established, optimizations of these methods were performed. Below are some results about the growth of HfGeO used in demo 2 and demo 3.

We have grown the **heterostructure** HfO_2 gate/Ge-HfO_2 intermediate/HfO_2 bottom/(100) Si, aiming to increase the efficiency on the wafer of structures with targeted ferroelectric properties. The first layer is the dielectric gate of the graphene channel, the second is the ferroelectric, while the third acts as barrier for the carriers of the doped substrate. In order to optimize the structure, RTA treatments were modified by slightly varying both the annealing temperature (600 ±15 ^oC) and the duration. As a result, the structures show much better ferroelectricity when d_{top} = 22 nm, d_{int} = 5 nm and d_{bot} = 7.3 nm (see Fig. 3.1). In Figs. 3.1(a) and (b), HRTEM images of the 3-layer structure are taken on a XTEM specimen. In Fig. 3.1(b), both orthorhombic (111) $HfO_{2,o}$ (in the intermediate layer) and monoclinic (100)

$HfO_{2,m}$ (in the top layer) are evidenced. In Fig. 3.2, remanent polarization loops as function of the applied bias (for 8 V and 9 V maximum biases) are shown. The total remanent polarization $2P_r$ (at 0V) is very close to the one found before (Stage 4), i.e. 6.5 ± 0.2 μC/cm² for pulses of ±10 V/5 s.

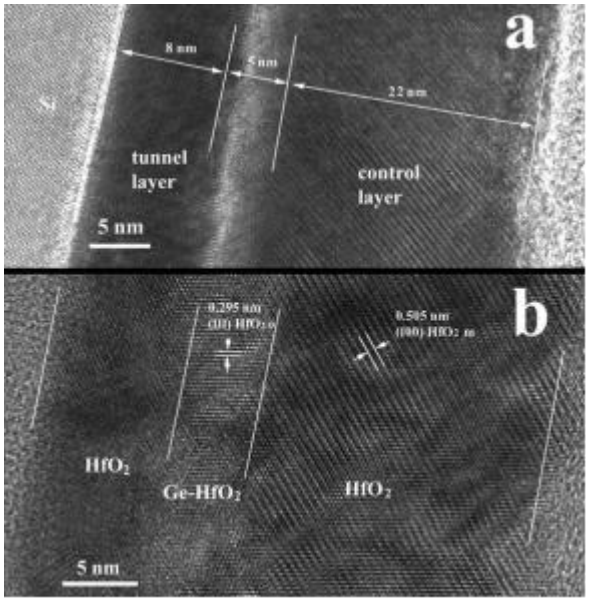


Fig. 3.1 HRTEM images of the trilayer heterostructure HfO_2 gate/Ge-HfO_2 intermediar/HfO_2 bottom/

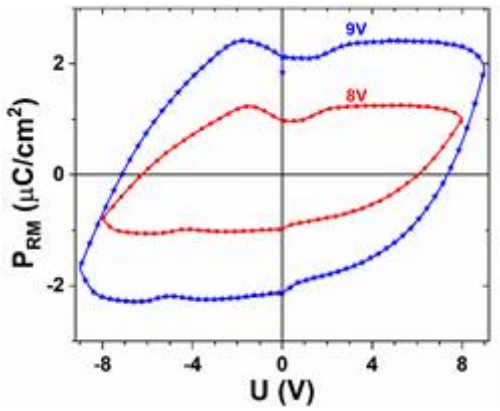


Fig.3.2 The P(U) curve.

Implementation of the task 3.2: The reconfigurable in-memory logic gate based on the graphene/ferroelectric heterostructure – demo2

The implementation of the reconfigurable logic gate is based on a three-gates configuration chosen for our graphene/HfGeO FETs, with two top gates and one backgate, which allows a single FET to act as several logic gates, depending on the voltages applied to the gates and the choice of current threshold. The fabrication process is depicted below (Fig.3.3):

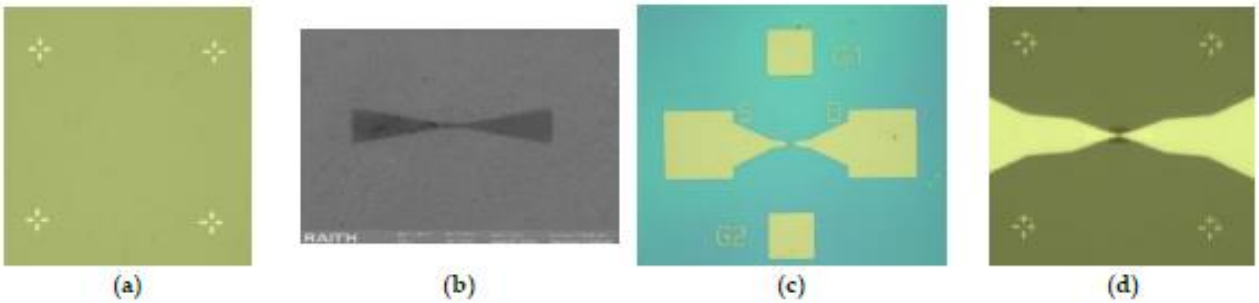
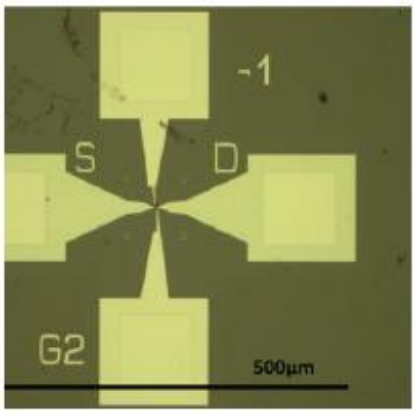
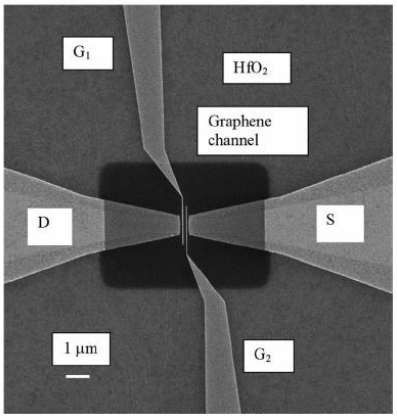


Fig.3.3 Optical images of the following fabrication steps: (a) alignment marks fabrication, (b) patterning using e-beam lithography, (c) source and drain contacts fabrication by e-beam, and (d) gate insulator deposition

The fabrication is made on the wafer grown in the previous task after the graphene monolayer was transferred on the entire wafer by Graphenea, Spain. The SEM image and the optical images of the three-gate FET are shown in Fig. 3.4. The channel length of the FET is 450 nm, its width is 800 nm and the distance between the two top gates is 150 nm.



(a)



(b)

Fig. 3.4 (a) Optical image and (b) SEM image of the three-gate FET playing the role of the reconfigurable logic gate (note that the third gate is the bottom gate which is the doped Si substrate).

The **electrical characterization** of graphene FETs was performed at room temperature using a Keithley SCS 4200 station. The probe station for wafer measurement is placed inside a Faraday cage, and all electrical channels are connected with low-noise amplifiers to the station. The probe station is equipped with mechanical devices dedicated to attenuate mechanical vibrations and shocks. All 200 transistors were measured and we have seen that 70% of them have worked in a reproducible manner, while the rest had various problems generated by bad metallic contacts, incomplete deposition and/or graphene defects. A typical dependence of the drain current, I_D, versus drain voltage, V_D, at various top gate voltages, V_{G1} and V_{G2}, is represented in Fig. 4, while the back-gate voltage (V_{BG}) is disconnected (Fig. 3.5).

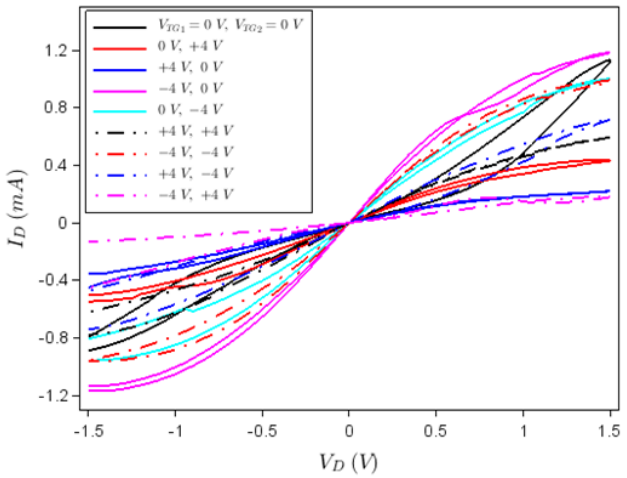


Fig. 3.5 I_D-V_D dependence if V_{G1} and V_{G2} are connected while V_{BG} is not connected

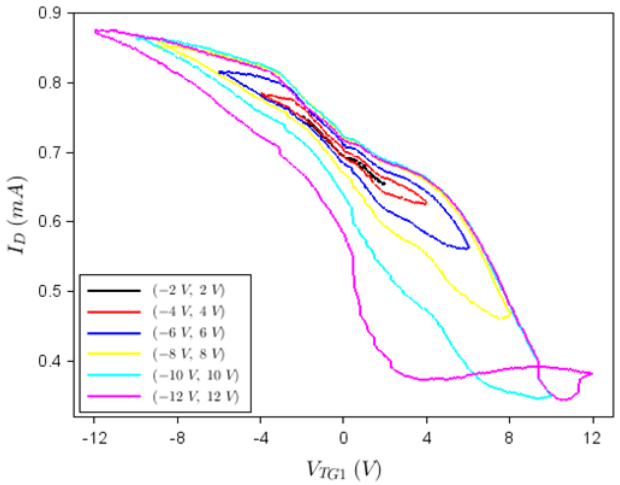


Fig.3.6 I_D-V_{G1} dependence while the other gates are not connected

In fact, Fig. 3.5 shows that the device acts as a memtransistor, i.e., a transistor with memory, due to the hysteretic clockwise behaviour of the I_D-V_D dependence at various top gate voltage values, the current in the forward drain voltage sweep (from 0 to 1.5 V) being higher than in the backward direction sweep (from 1.5 V to 0). This hysteretic behaviour is due mainly to charge storage in the Ge nanocrystals in the intermediate layer A confirmation of the fact that we are dealing with a memtransistor is the I_D-V_{G1} dependence illustrated in Fig. 3.6 and obtained by disconnecting the other gates; this last figure shows that this transistor has a non-volatile memory conferred by the ferroelectric HfGeO. Similar results were obtained with any other gates of the memtransistors.

The graphene monolayer/ferroelectric FET is a voltage-controlled transistor with a ferroelectric floating gate, i.e., the drain current is controlled by the gate voltages applied up and down the channel. In the case of 2D monolayer materials, as in our situation, the drain current is only a surface current, which can be effectively controlled by the top- and back-gate voltages. On the other hand, the ferroelectric floating gate confers memory properties to the same transistor. Thus, we find in a single device two functionalities: reconfigurability of digital logic gates, which can be implemented, and non-volatility of these logic gates until new gate voltages are applied. The working of the memristor as reconfigurable logic gate can be understood with respect to the I_D-V_D characteristics in Fig. 3.5. In this respect, the gates are programmed to have the values +4 V, -4 V and 0 V. The input for a logical gate level is considered as logic "0" if no voltage is applied, irrespective of the gate type, the logic value 1 being attributed otherwise. The output is encoded in I_D (in the forward direction) for a drain voltage of 1 V; if we consider as reference/threshold the drain current level when $V_{G1} = V_{G2} = 0$ V, the drain current value above this threshold is associated to logic value 1, while the value below it is defined as logic value 0. Then, we have the logic table displayed as Table 3.1; the threshold drain current values for the OR and AND gates is 0.5 mA, whereas for XOR the corresponding value is 0.4 mA.

On the other hand, if we select the level (-4 V, +4 V) as 0 because it produces the lowest value of I_D (below these gate voltages the transistor is OFF), we obtain a NAND gate, the functioning of which is detailed also in Table 3.1; for this logic gate the threshold value for I_D is 20 mA. NAND is a universal gate, in terms of which any logical gate or function can be expressed, and thus it is very important to implement it. All these results are obtained for two logical inputs (top gates) and one logical output – the drain current. Other logic gates can be implemented in this way. Similar results are obtained using a back gate and a top gate, for example V_{G1} and V_{BG}, while the other top gate is disconnected. Analogously, if we consider the drain current value at a certain drain voltage at $V_{G1} = V_{BG} = 0$ V as 0 logic, we can also configure various logic gates as in the examples above.

Table 3.1. Logic tables for different functions and their implementation. The inputs are written as (V_{G1}, V_{G2} in [V])/logic values while the output is the logic value of I_D

OR		AND		XOR		NAND	
inputs	output	inputs	output	inputs	output	inputs	output
(0,0)/(0,0)	0	(0,0)/(0,0)	0	(0,0)/(0,0)	0	(-4,+4)/(0,0)	1
(0,-4)/(0,1)	1	(0,+4)/(0,1)	0	(0,-4)/(0,1)	1	(0,-4)/(0,1)	1
(-4,0)/(1,0)	1	(+4,0)/(1,0)	0	(-4,0)/(1,0)	1	(-4,0) /(1,0)	1
(-4,-4)/(1,1)	1	(-4,-4)/(1,1)	1	(-4,+4)/(1,1)	0	(-4,-4)/(1,1)	0

These FETs are termed as neuristors since a single device is able to perform logical operations such as OR, AND and XOR, like a single cortex neuron [23]. Also, transistors such as these, which are able to perform different logical tasks as programmed, were referred to as adaptable or intelligent [24].

Implementation of the task 3.3: The memtransistor - the electronic analogue of a neuronal synapse – demo 3

We have shown that graphene/HfZrO FETs are memtransistors when the graphene is transferred on the ferroelectric HfO_2/Ge-HfO_2/HfO_2 3-layers-structure. In principle, memristors are two-terminal devices, which are resistive non-volatile memories having two distinct states *on* and *off* displaying a time evolution formed by repetitive hysteresis loops of current-voltage dependence. They are the electronic analogue of a synapse, since their conductance is modulated by charges and mimics spike timing dependent plasticity [25]. Two-terminal memristors are represented mainly by valence change memristors (VCM) or filament memristors, which are metal-insulator-metal (MIM) structures where the insulator is an oxide such as TiO_x, HfO_x, or a 2D material. Memtransistors are active three-terminal devices based on FETs, having clear advantages over two-terminal memristors: (i) no electroforming process for the wake-up, (ii) tunable memory functions, (iii) high on-off ratios, and (iv) no sneak paths in crossbar arrays. Any memtransistor is an artificial synapse. The first memtransistors were fabricated on flakes of MoS_2, but the drain voltage was 80 V and, although it reduced progressively up to 12 V using different methods, remained still too high to be used in neuromorphic applications. In contrast, our ferroelectric memtransistors based on HfO_2/Ge-HfO_2/HfO_2 3-layers-structure are working at drains voltages in the range of -2 to +2 V and are fabricated at the wafer level (for more references please see M. Dragoman, et al. Wafer-scale graphene-ferroelectric HfO_2/Ge-HfO_2/ HfO_2 transistors acting as three-terminal memristors, Nanotechnology 31, 495207 (2020)). In Fig. 3.7 we present the cross-section of the HfO_2/Ge-HfO_2/HfO_2 FET memtransistor, while in Fig. 3.8 the array of 250 transistors fabricated on the same chip is represented.

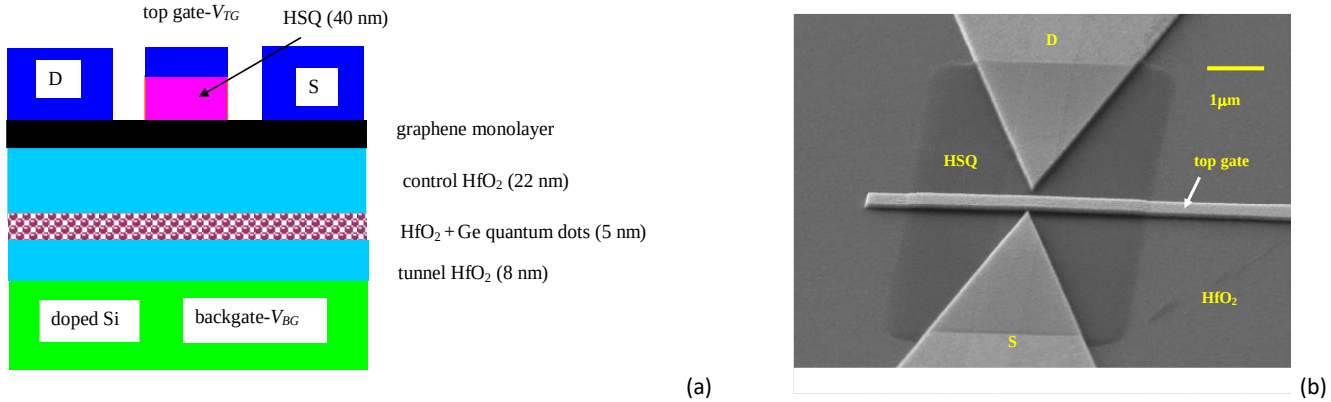


Fig. 3.7 The graphene/ HfO_2/HfGeO/ HfO_2/Si memtransistor: (a) cross-section, and (b) SEM image

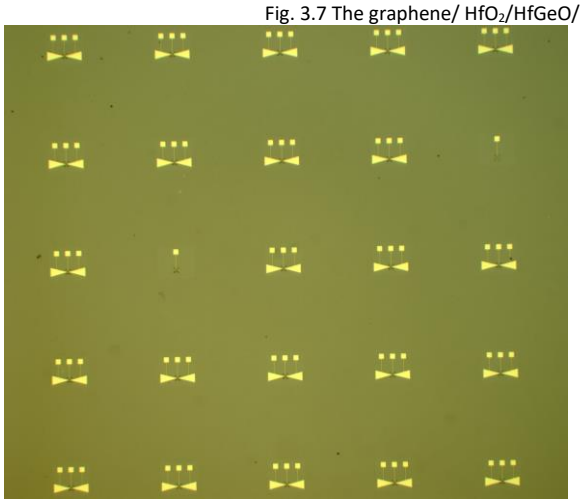


Fig. 3.8 The optical image of the ferroelectric HfO_2/Ge-HfO_2/HfO_2 FET memtransistors chip.

The fabrication of FETs is performed in several standard steps. First, the graphene channel is patterned using e-beam lithography (Raith e_Line at 30 kV) and then etched using oxygen plasma (the etching time is 3 s using SENTECH Instruments SI 220). The second step is dedicated to source (S) and drain (D) contacts patterning, metallization, and lift-off. The electrodes are Ti/Au (5/35 nm) and are deposited by e-beam evaporation (TEMESCAL FC2000). The third step consists of the deposition of the top gate dielectric HSQ having 40 nm thickness, while the last step is top gate metal deposition of Ti/Au (5/145 nm) using e-beam evaporation (TEMESCAL FC2000).

The DC performances of the transistors were measured using a Keithley SCS 4200 station in the same way as for demo 2 described above. Any ferroelectric memtransistor has two main functions. First, it works like a three-terminal memristor when we consider the drain current (I_D) versus drain voltage (V_D) at various top-gate voltages (V_{TG}) and back-gate voltage (V_{BG}). In Fig. 3.9(a) we have represented I_D versus V_D at various top gate voltages when the V_{BG} = 0, while in Fig. 3.9(b) we have represented the dependence I_D-V_{TG} for different back-gate voltages V_{BG}, for V_D = 1 V. All the dependencies show hysteretic behavior in the clockwise direction.

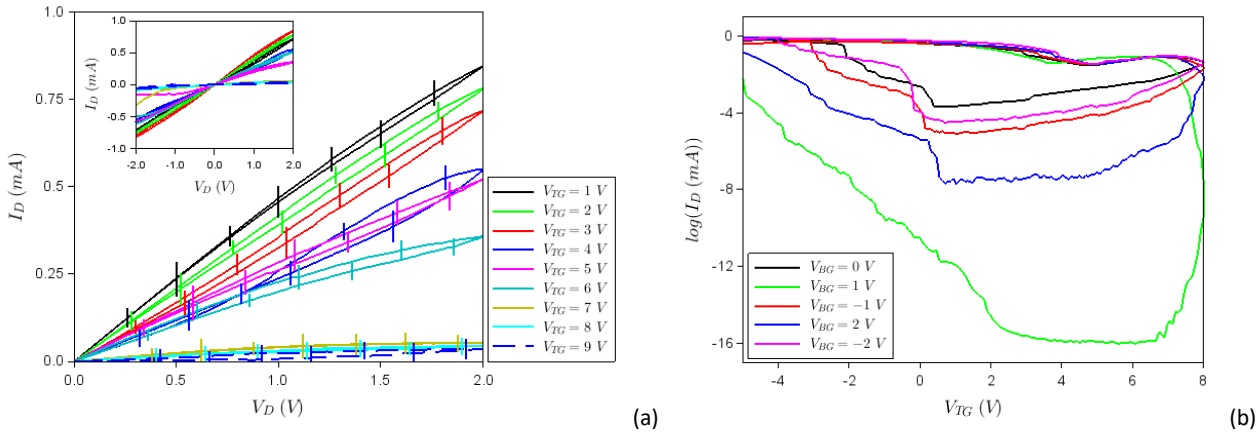


Fig. 3.9 (a) I_D versus drain voltage (V_D) at various top-gate voltages (V_{TG}) (b) I_D-V_{TG} for different back-gate voltages V_{BG} on a semi-logarithmic scale.

We see in the above figure the unique imprint of any memtransistor, i.e., a rotating hysteresis at various gate voltages. The error bar is considered from the measurements of 7 devices. Looking at the same dependence in the logarithmic scale we see that there are 12 orders of magnitudes between an *off* state (at V_{TG} = 9 V) and an *on* state (at V_{TG} = 1 V), so the memtransistors are performant switches.

The effect of backgate voltage variation is significant for both *on* and *off* states of memtransistors, defined in this case as states with low and high resistances for opposite sweeps of the top gate. Thus, if at V_{BG} = 0, there are more than three orders of magnitude difference between the *on*-state current defined in forward V_{TG} sweep and the *off*-state drain current in the backward sweep at V_{TG} = +2 V, the corresponding ratio increases with orders of magnitude for V_{BG} = +2 V and even more for V_{BG} = +1 V. For this latter back-gate voltage value, the floating gate is blocking the flow of current in the graphene monolayer channel for the backward sweep of V_{TG}, enhancing thus dramatically the ratio between the *on* and *off* currents. The memtransistor displays a memory window in the range 5-8 V depending on the applied V_{TG}. In Fig. 3.10 we have represented a typical I_D dependence in time at different sweeps when the drain voltage is +2 V (top) and -2 V (bottom). We see that when the number of sweeps is increased, the current is saturated. This behaviour is the electrical analogue of the non-associative learning mechanisms termed habituation, dishabituation and memory. When the conductance is increasing (decreasing) in time the habituation mechanism is acting, and after a while the stimulus (the applied voltage) is learned and memorized.

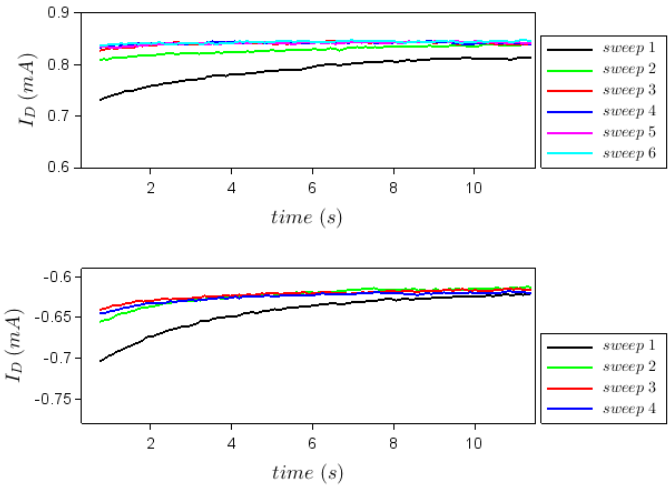


Fig. 3.10 The drain current dependence in time for a drain voltage of +2 V (top) and −2 V (bottom).

Conclusions for the objective 3

The goals of the objective 2 (demo 2 and demo 3) were accomplished at the end of 2021 and represent the state of the art advances in the area of neuromorphic devices.

4 Implementation of the Objective 4 (2022 -6 months): Thermoelectric devices based on graphene/ferroelectric heterostructures – demo 4

This last objective has the following tasks:

4.1 The growth of HfO_2-based ferroelectrics

4.2 The simulation of the thermoelectric graphene/ferroelectric heterostructures

4.3. The fabrication and measurements of graphene/ferroelectric heterostructures.

Implementation of the task 4.1: The growth of HfO_2-based ferroelectrics

We have grown HfZrO using ALD, HfGeO using magnetron sputtering, and PZT via PLD, but the best results in the case of thermoelectric applications are obtained for HfZrO ferroelectrics. Since the growth methods were well established, only optimizations of these methods were performed in the last six months of the project. Moreover, knowing that the ferroelectric properties are deteriorating during time, we have made a reliability measurement of HfZrO grown this year and one year ago under the same conditions and on the same equipment.

The top electrode for all devices is Cr (5 nm)/Au (100 nm), with dimensions 150 μm×150 μm, while the bottom electrode is doped Si. The measurement results are represented in Fig. 4.1.

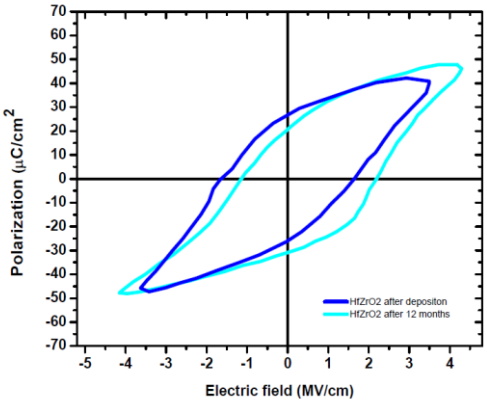


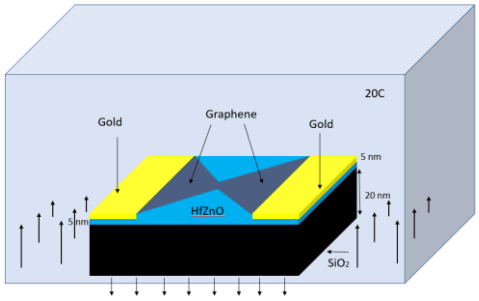
Fig. 4.1 $P(E)$ for HfZrO now and one year ago.

From these results it follows that $2P_r$, which is the sum of the polarizations on the positive (+) and the negative (-) axes, changes with only 2% in one year. Regarding the coercive electric field, we observe that the asymmetry is more pronounced, producing a shift of *P*(*E*) but almost preserving the shape of the curve. These results show that HfO_2-based ferroelectrics are stable during time. Similar results are obtained for other HfO_2-based ferroelectrics, doped with Al or Ge.

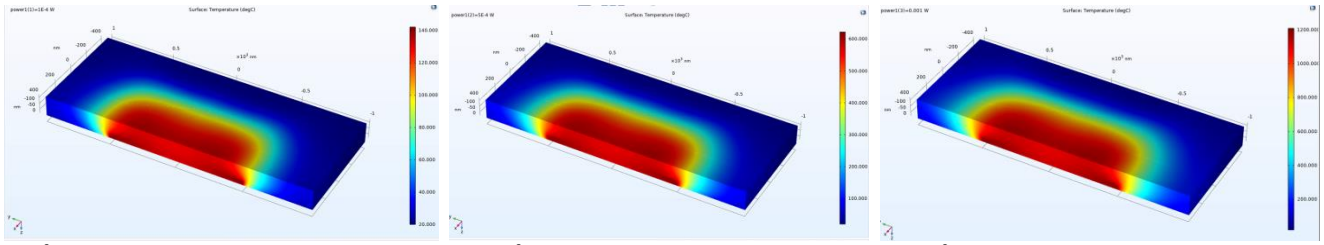
Implementation of the task 4.2: The simulation of the thermoelectric graphene/ferroelectric heterostructures.

Thermoelectricity means the generation of a DC voltage as a result of a temperature difference produced in a device, i.e., $V = S\Delta T$ where S is the Seebeck coefficient. We have chosen two types of devices able to produce DC voltages due to a temperature gradient ΔT . The first category of devices are FET graphene/ferroelectrics transistors, where the channel is nonuniform, i.e., has the shape of a bowtie, or letter Δ since the geometrical nonuniformity of the channel is enhancing ΔT in these structures [26]. The second thermoelectric device is a microwave FET, where the gate is the hot electrode while the massive source electrode is the cold electrode (M. R. Gasper et al., Thermoelectric graphene nanoconstrictions as detector of microwave signals, IEEE Trans. Nanotechnology 18, 879-884 (2019)). We have simulated both categories of devices using COMSOL. Many interesting aspects were revealed, but we will present here only the main results.

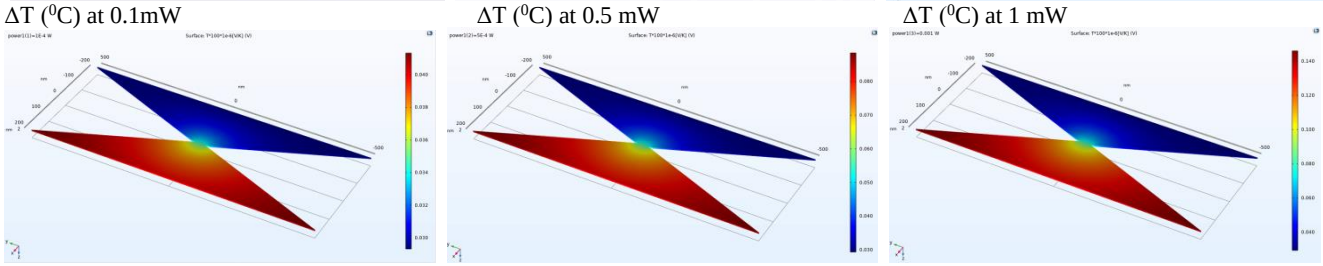
The simulated model of a bow-tie non-uniform graphene channel FET (the bottom electrode is doped Si, playing the role of a back-gate) is represented in Fig. 4.2(a). If we consider that the non-uniform graphene channel thermal conductivity is 300 W/mK we have the following results at various thermal powers applied on one electrode using COMSOL-Heat Conjugate Transfer displayed in Fig. 4.2(b).



(a)



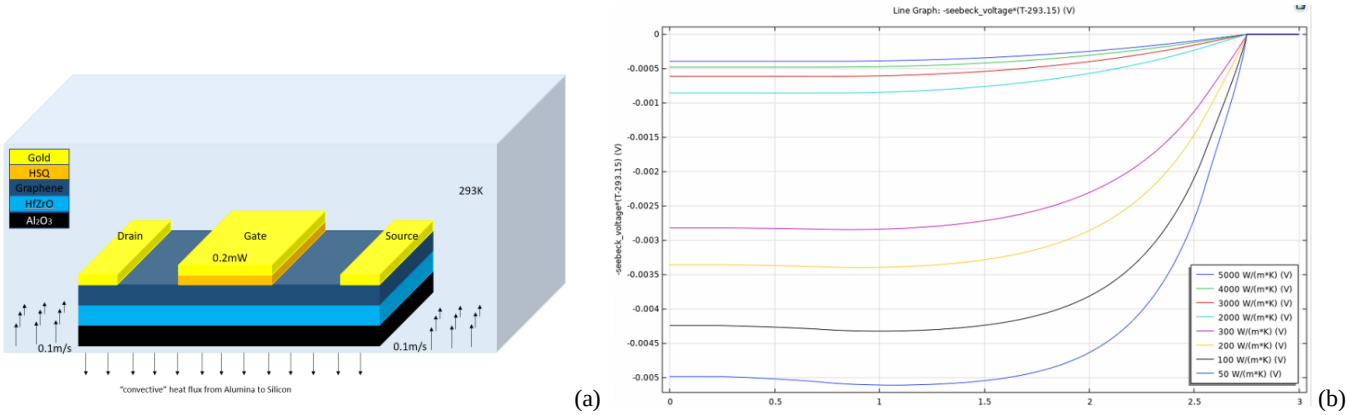
ΔT (^{0}C) at 0.1mW ΔT (^{0}C) at 0.5 mW ΔT (^{0}C) at 1 mW



thermoelectric V (V) at 0.1mW thermoelectric V (V) at 0.5mW thermoelectric V (V) at 1mW (b)

Fig. 4.2 (a) The simulated model of a bow-tie non-uniform graphene channel FET and
(b) DC voltages produced at various thermal powers applied on one electrode.

The microwave model is depicted below, in Fig. 4.3(a), while the thermoelectric voltage distribution along the channel is displayed in Fig. 4.3(b), when the Seebeck coefficient is around 100 μV/K.

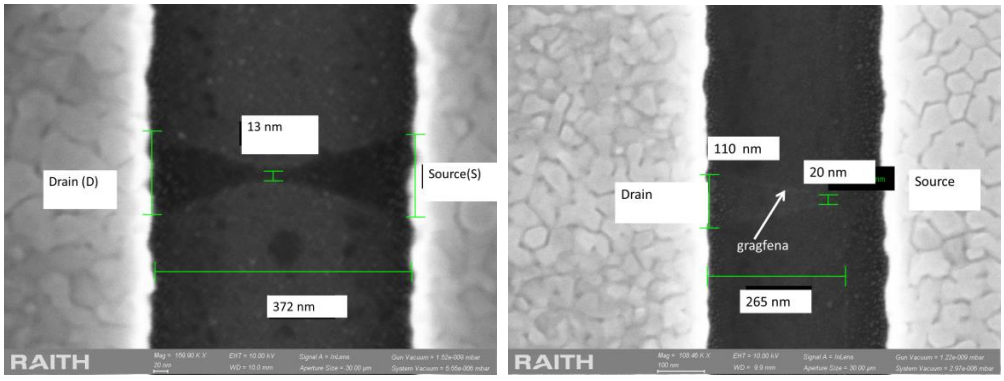


(a) (b)

Fig. 4.3 (a) The microwave model and (b) the thermoelectric voltage distribution along the channel when the input power is 0.2 mW.

Implementation of the task 4.3: The fabrication and measurements of graphene/ferroelectric heterostructures.

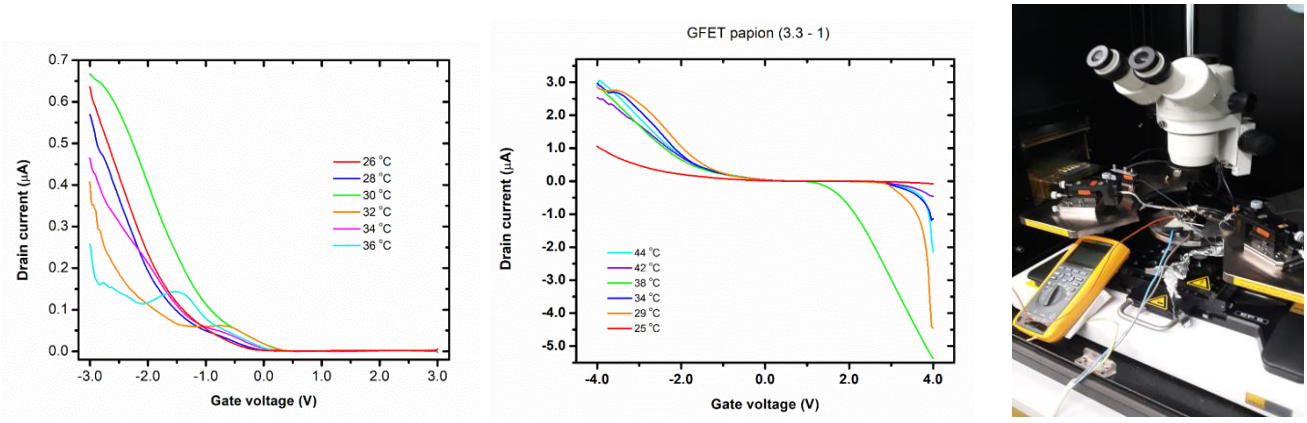
First, we have fabricated the FETs with a nonuniform graphene channel. The fabrication is identical with that used for other demonstrators and will not be repeated here. In Fig. 4.4 we have displayed the SEM image of the two types of FET having nonuniform graphene channels.



(a) (b)

Fig.4.4 The SEM image of the FET having the channel shape (a) bowtie(b) Δ graphene

We have then heated the chips of the above FETs in the range 25-50 ^{0}C with a mini-heater place below the chip (see the set-up image in Fig. 4.5). The I_D-V_G dependences in temperature of the two types of FETs are represented in Figs. 4.5(a) and (b), respectively.



(a) (b) (c)

Fig. 4.5 I_D-V_G dependence in temperature of a FET with the channel shaped as (a) the letter Δ and (b) bowtie. (c) The measurement set-up.

In the case of the FET with a channel shaped as a bowtie, we can see that the S value, of - 200 μV/K, is obtained at V_G = +4 V at 38 ^{o}C. This value of the Seebeck coefficient is an order of magnitude larger than in the case when the channel has the shape of the letter Δ. Moreover, at negative gate voltages, for instance at V_G = -4 V and at 4 K temperature difference compared to room temperature, S is +320 μV/K. At zero drain voltage and at 4 K temperature difference compared to room temperature, the thermoelectric voltage is 0.3 mV.

The designed and fabricated thermoelectric microwave detector are presented in Figs. 4.6 and 4.7, respectively. The structure is a top-gate FET with a nanopatterned graphene monolayer channel. The measurement set-up of the detector at room temperature is presented in Fig. 4.8, while in Fig. 4.9 we can see the setup for thermoelectric measurement in the temperature range 100-200 K.

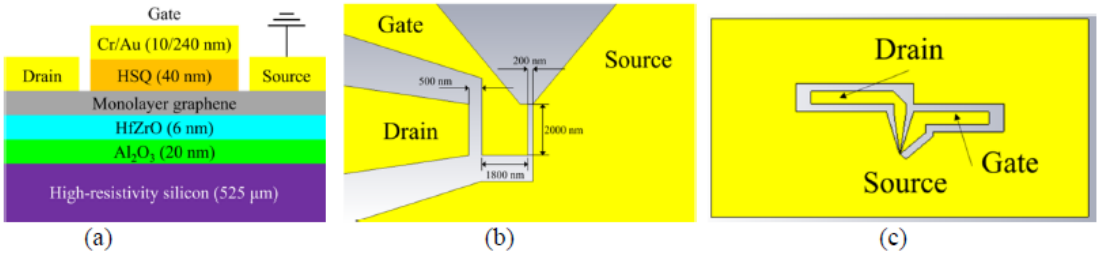


Fig. 4.6 (a) Cross-section, (b) gate details, and (c) coplanar microwave electrodes of the FET.

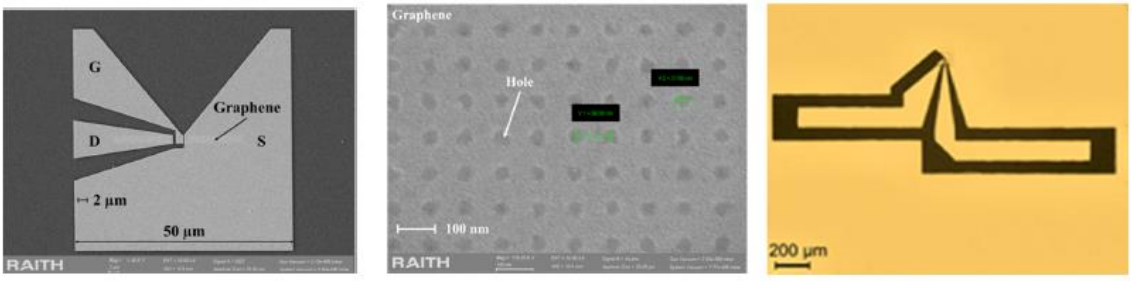


Fig. 4.7 (a) SEM image, (b) the nanopatterned graphene channel, and (c) optical image with transistor electrodes

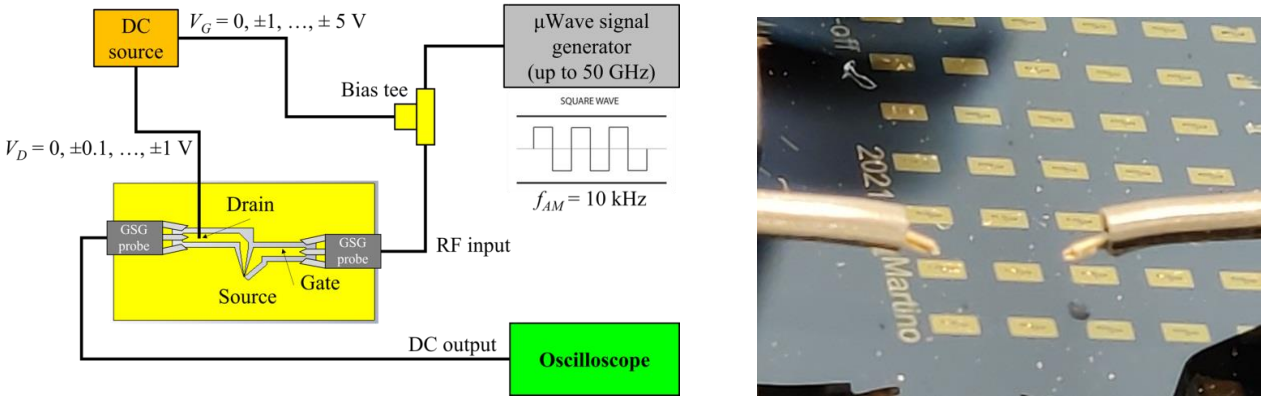


Fig. 4.8 Thermoelectric measurement at room temperature

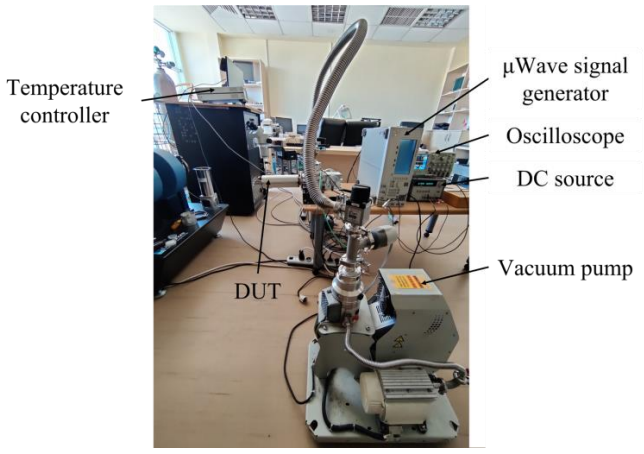


Fig. 4.9 The thermoelectric measurement setup in the temperature range 100-200 K.

The FET is working at zero drain voltage, i.e., there are no carriers in the cannel, while through the top gate microwave pulses are pumped in the circuit. The detected thermoelectric drain voltage at room temperature is shown in Fig. 4.10. In Fig. 4.11 we show the thermoelectric voltage at 100 K at various input microwave powers.

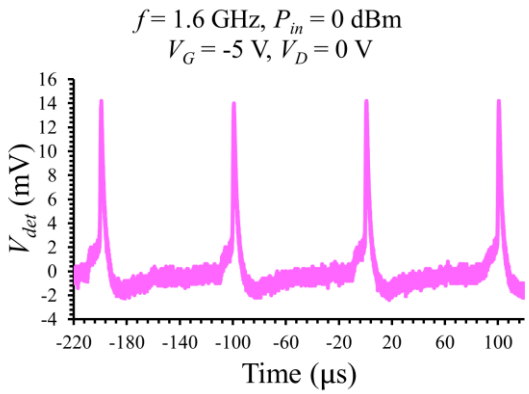


Fig. 4.10 The thermoelectric detected voltage at room temperature

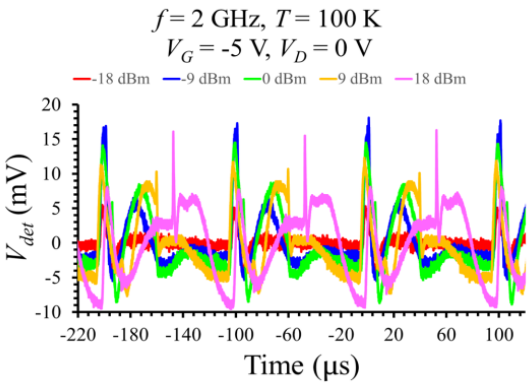


Fig. 4.10 The thermoelectric detected voltage at room temperature

In Fig. 4.12 we have represented the dected DC voltages and responsivities of the thermoelectric microwave photodector at various frequencies and microwave powers. The responsitivities around 100 V/W for a thermoelectric detector are rather hight. The linearity of detected voltage is a clear imprint of the thermoelectric signal, since increasing the power ΔT is increasing also, but at the negative gate voltage of -5 V the Seebeck coeffcient is negative, of -210 μV/K; this is a similar value as that calculated for graphene/ferroelectric FETs with a nonuniform channel. Thus, the detected voltages decrease linearly with the input power.

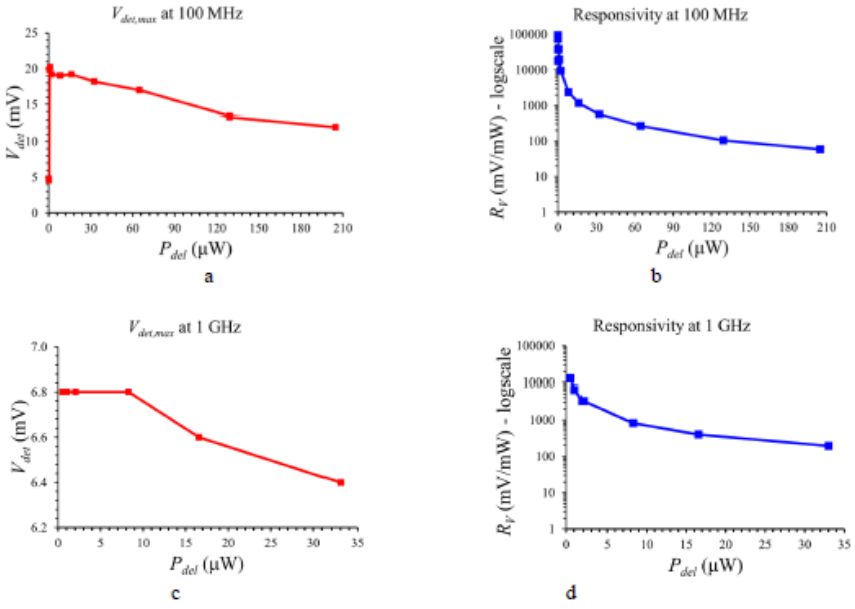


Fig. 4.12 The detected DC voltages and responsivities at 100 MHz and 1 GHz.

Conclusions

We have successfully implemented all the objectives of the project. The above results are at the state-of-the-art level, and all demonstrators are beyond the state of the art, each of them being a novelty in nanoelectronics. This statement is sustained by the publications resulted from this project, which are listed below. We have been invited with **2 invited talks** about this project at EMRS and two invited reviews were written about this project:

1. **M. Dragoman, M. Aldrigo, D. Dragoman, S. Iordanescu, A. Dinescu, M. Modreanu, HfO_2-based Ferroelectrics Applications in Nanoelectronics, Physica Status Solidi Rapid Research Letters, https://doi.org/10.1002/pssr.202000521 (2021).**
2. **M. Dragoman, M. Aldrigo, D. Dragoman, S. Iordanescu, A. Dinescu, M. Modreanu, The rise of ferroelectricity at nanoscale, Nanotechnology Magazine, vol. 15, pp. 8-19 (2021).**

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Results indicators

Indicators	Description / Name
Articles published/accepted/under evaluation in ISI indexed journals	*Article title/Year/DOI/ISSN or eSSN/Journal/Authors/Status(under evaluation/accepted/published)* 1. Electromagnetic interference shielding in X-band with aero-GaN, 2019, https://doi.org/10.1088/1361-6528/ab2023, NANOTECHNOLOGY, - M. Dragoman, T.B Tudor, S. Iordanescu, A. Martino, R. Simion, S. Sindu, R. Adelung, I. Tighineanu –published. 2. Integration of Antenna Array and Self-Switching Graphene Diode for Detection at 28 GHz, 2019, DOI: 10.1109/LED.2019.2899028, IEEE TRANSACTIONS ON ELECTRON DEVICES LETTERS, M. Yasir, A. Martino, M. Dragoman, B. Maurizio, A. Dinescu, S. Iordanescu, D. Vasilache – published. 3. Graphene bandgap induced by ferroelectric Pca21 HfO2 substrate: a first-principles study, 2019, https://doi.org/10.1039/C9CP01786K, PHYSICAL CHEMISTRY CHEMICAL PHYSICS, - G. A. Nemneş, D. Dragoman, M. Dragoman – published. 4. Terahertz shielding properties of aero-GaN, 2019, https://doi.org/10.1088/1361-6641/ab4e58, SEMICONDUCTOR SCIENCE AND TECHNOLOGY, B. Tudor, Z. Segey, M. Dragoman, A. Liudmila, V. Ciobanu, A. Martino, D. Dragoman, S. Iordanescu, S. Sandu, R. Simion, A. Rainer, I. Tighineanu – published. 5. Orthorhombic HfO_2 with embedded Ge nanoparticles in nonvolatile memories used for the detection of ionizing radiation, 2019, https://doi.org/10.1088/1361-6528/ab352b, NANOTECHNOLOGY, C. Palade, A. Slav, A. M. Lepadatu, I. Dascalescu, M. V Maraloiu, C. C Negrila, C. Logofatu, T. Stoica, S. V. Teodorescu, V. Serban, M. Ciurea, S. Lazanu –published. 6. Low-voltage permittivity control of coplanar lines based on hafnium oxide ferroelectrics grown on silicon, 2020, DOI/10.1109/ACCESS.2019.2942430, IEEE Access, A. Martino M. Dragoman, S. Iordanescu, F. Nastase, S. Vulpe, A. Dinescu – published. 7. Wafer-scale graphene-ferroelectric HfO2/Ge–HfO2/HfO2 transistors acting as three-terminal memristors, 2020, https://doi.org/10.1088/1361-6528/abb2bf, NANOTECHNOLOGY, M. Dragoman, A. Dinescu, D. Dragoman, C. Palade, A. Moldovan, M. Dinescu, V. S. Teodorescu, M. Ciurea –published. 8. Graphene bandgap induced by ferroelectric HfO2 doped with Zr (HfZrO), 2020, https://doi.org/10.1088/1361-6528/ab814b, NANOTECHNOLOGY, M. Dragoman, A. Dinescu, F. Nastase, A. Moldovan. D. Dragoman – published. 9. Memtransistors Based on Nanopatterned Graphene Ferroelectric Field-Effect Transistors, 2020, https://doi:10.3390/nano10071404, NANOMATERIALS, M. Dragoman, A. Dinescu, F. Nastase, D. Dragoman – published. 10. Tunable Microwave Filters Using HfO2-Based Ferroelectrics, 2020, https://doi:10.3390/nano10102057, NANOMATERIALS, M. Aldrigo, M. Dragoman, S. Iordanescu, F. Nastase, S. Vulpe – published. 11. Reconfigurable horizontal–vertical carrier transport in graphene/HfZrO field-effect transistors, 2020, https://doi.org/10.1088/1361-6528/ab4832, NANOTECHNOLOGY, M. Dragoman, M. Modreanu, I. Povey, A. Dinescu, D. Dragoman – published. 12. MoS2 radio: detecting radio waves with a two-dimensional transition metal dichalcogenide semiconductor, 2020, https://doi.org/10.1088/1361-6528/ab5123, NANOTECHNOLOGY, M. Dragoman, M. Aldrigo, J. Connolly, I. Povey, S. Iordanescu, A. Dinescu, D. Vasilache, A. Dinescu, D. Vasilache, M. Modreanu – published. 13. Perspectives on atomic-scale switches for high-frequency applications based on nanomaterials, 2021, https://doi.org/10.3390/nano11030625, NANOMATERIALS, M. Dragoman, M. Aldrigo, D. Dragoman – published 14. Bloch oscillations at room temperature in graphene/h-BN electrostatic superlattices, 2021, https://doi.org/10.1088/1361-6528/ac02e6,NANOTECHNOLOGY, M. Dragoman, A. Dinescu, D. Dragoman, F. Comanescu – published 15. HfO_2-based ferroelectrics applications in nanoelectronics, 2021, https://doi.org/10.1002/pssr.202000521, PHYS. STATUS SOLIDI RRL, M. Dragoman, M. Aldrigo, D. Dragoman, S. Iordanescu A. Dinescu, M. Modreanu – published 16. The rise of ferroelectricity at nanoscale, 2021, https://10.1109/MNANO.2021.3098217, IEEE NANOTECHNOLOGY MAGAZINE, M. Dragoman, M. Aldrigo, D. Dragoman, S. Iordanescu, A. Dinescu, M. Modreanu – published 17. Effects of Ge-related storage centers formation in Al2O3 enhancing the performance of floating gate memories, 2021, https://doi.org/10.1016/j.apsusc.2020.148702, APPL. SURF. SCI., I. Stavarache, O. Cojocaru,

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Books	*Title/Publishing year/Publishing house/ISBN* M. Dragoman, D.Dragoman, *Atomic scale electronics beyond CMOS*, Springer, 2021, ISBN 978-3-030-60563-6

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